EEE 3571 Electronic Engineering I

Lecture 2: Analog Electronics
Diode Applications

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References

Our main reference text books in this course are

[1] Neil S., Electronics: A Systems Approach, 4th edition, 2009, Pearson Education Limited, ISBN 978-0-273-71918-2.

[2] Boylestad R. L., Nashelsky L., Electronic Devices and Circuit Theory, 11th Ed, 2013, Prentice-Hall, ISBN 978-0-13-262226-4.

[3] Smith R. J., Dorf R. C., Circuits Devices and Systems, 5th Ed., 2004, John Wiley, ISBN ISBN 9971-51-172-X.

However, feel free to use pretty much any additional text which you might find relevant to our course.

Special Acknowledgement to Mr Jerry Muwamba for the original development of the PPT slides and to Dr Brilliant Habeenzu for building on them.

Learning Objectives

At the end of the lecture on diode application, you ought to:

1. Understand the concept of load-line analysis and how it is applied to diode networks.
2. Become familiar with the use of equivalent circuits to analyze series, parallel, and series-parallel diode networks.
3. Understand the process of rectification to establish a dc level from a sinusoidal ac input.
4. Be able to predict the output response of a clipper and clamper diode configuration.
5. Become familiar with analysis of and the range of applications of Zener diodes.

2.1 Introduction

- In this lecture the fundamental behavior pattern of diodes in dc and ac networks will be brought to the fore and ought to be clearly understood.
- The concepts learned in this lecture are of primary importance to in the lectures to follow.
- In general, the analysis of electronic circuits can follow one of the two paths: using the actual characteristics or applying an approximate model for the device.
- For the diode the initial discussion will include the actual characteristics to clearly demonstrate how characteristics of a device and network parameters interact.
- Most importantly the role and response of various elements of an electronic system will be understood without continually having to resort to lengthy and rigorous mathematical procedures.

2.1 Load-line Analysis

- The circuit of Fig. 2.1 will be used to describe the analysis of a diode circuit using its actual characteristics.
- Thus, solving the circuit in this case entails finding the current and voltage levels that will satisfy both the characteristics of the diode and the chosen network parameters simultaneously.

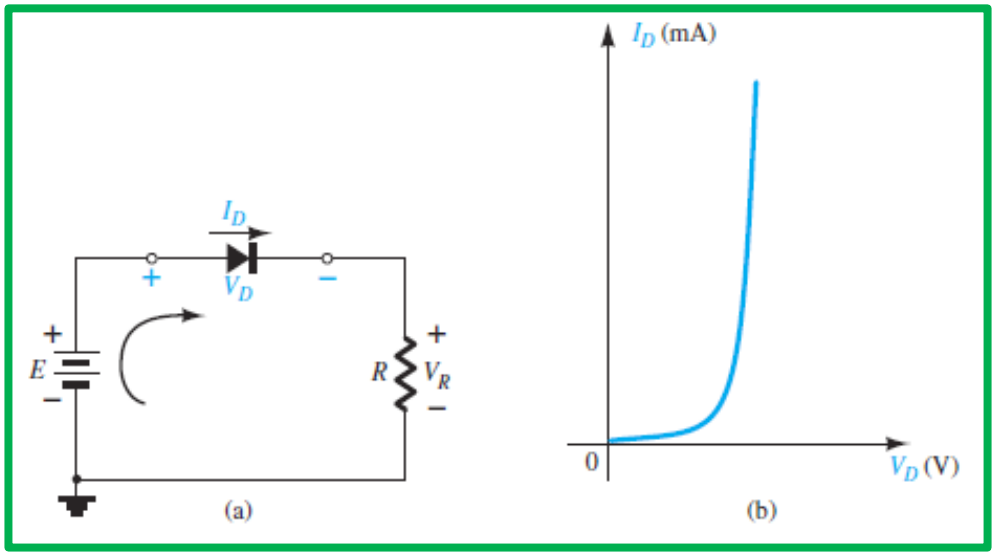


Figure 2.1: Series diode configuration: (a) circuit; (b) characteristics.

2.1 Load-line Analysis Cont'd

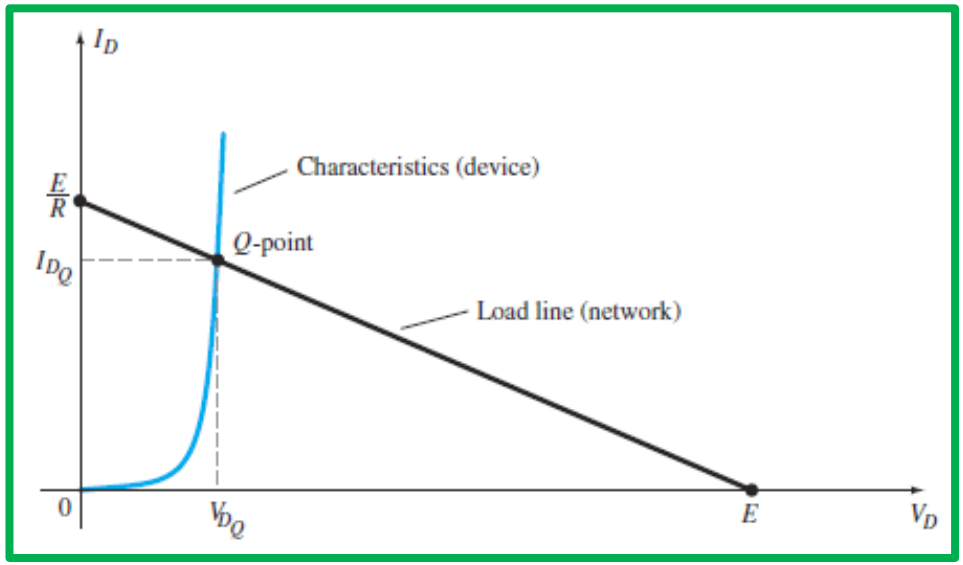


Figure 2.2: Drawing the load line and finding the point of operation.

- Fig. 2.2 shows the diode characteristics placed on the same axes as a straight line defined by the parameters of the network.
- The straight line is called a load line since the intersection on the vertical axis is defined by the applied load *R*.
- Thus, the load line analysis will follow.

- Applying Kirchhoff's voltage law (KVL) in the clockwise direction of the ckt in Fig. 2.1 yields

$$E - V_D - V_R = 0; \qquad \therefore\ E = V_D + I_D R \qquad \textbf{[2.1]}$$

2.1 Load-line Analysis Cont'd

- The two variables of Eq. [2.1], V_D and I_D, are the same as the diode axis variables which permits co-plotting the two curves in Fig. 2.2.
- Thus, the operating point is easily determined if one simply employs the fact that anywhere on the horizontal axis $I_D = 0\,\text{A}$ and anywhere on the vertical axis $V_D = 0\,\text{V}$.
- Letting $V_D = 0\,\text{V}$ in Eq. [2.1] and solving for I_D yields

$$E = V_D + I_D R; \;\Rightarrow\; E = 0 + I_D R;$$

$$I_D = \left.\frac{E}{R}\right|_{V_D = 0\,\text{V}} \qquad [2.2]$$

- Similarly, by letting $I_D = 0\,\text{A}$ in Eq. [2.1] and solving for V_D yields

$$E = V_D + I_D R; \;\Rightarrow\; E = V_D + (0)R;$$

$$V_D = \left. E \right|_{I_D = 0\,\text{A}} \qquad [2.3]$$

2.1 Load-line Analysis Cont'd

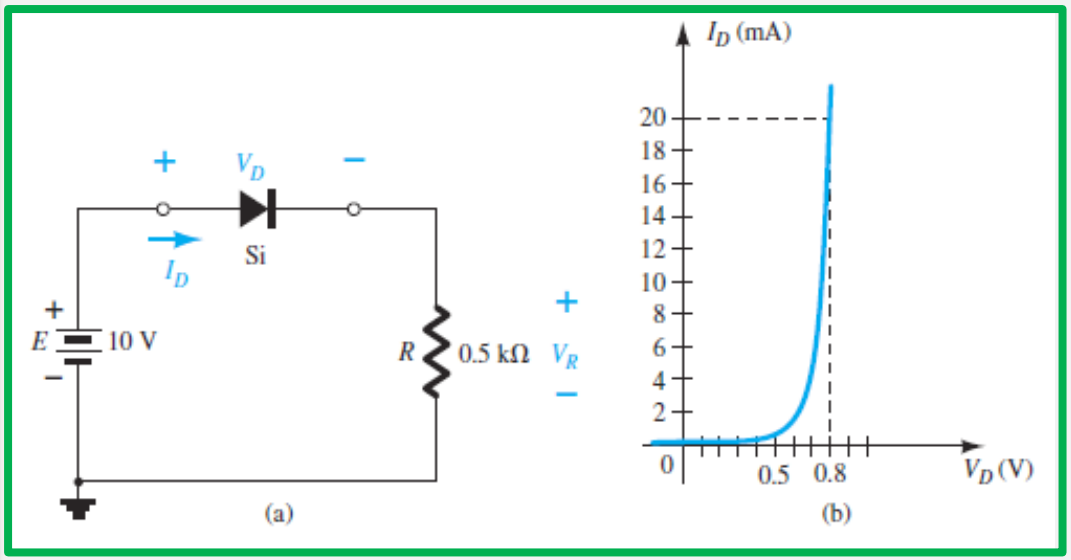
- Thus, a straight line drawn between the two points found in Eq. [2.2] and [2.3] defines the load line as depicted in Fig. 2.2.
- Vividly, changing the load, *R* changes the intersection on the vertical axis and essentially changes the intersection (operating point).
- The operating point is often called the **quiescent point (*Q*-point)** to reflect its "still, unmoving" quantities as defined by a dc network.
- At the *Q*-point (intersection) by simply drawing a vertical line down to the horizontal axis yields the diode voltage V_{D_Q} and a horizontal line gives the current I_{D_Q}.
- Alternatively, the *Q*-point voltage, V_{D_Q} and current, I_{D_Q} would be obtained by solving the simultaneous equations below mathematically.

$$I_D = \frac{E}{R} - \frac{V_D}{R}$$ [derived from Eq. [2.1]]

[2.4]

$$I_D = I_s\left(e^{V_D/nV_T} - 1\right)$$

Example 2.1 Load-line Analysis



- For the series diode configuration of Fig. 2.3a, employing the diode characteristics of Fig. 2.3b, determine:

a) V_{D_Q} and I_{D_Q}.

b) V_R .

Figure 2.3: (a) Circuit; (b) characteristics.

[Solution]

a) Eq. [2.2] yields:

$$I_D = \frac{E}{R}\bigg|_{V_D=0\,\mathrm{V}} = \frac{10\,\mathrm{V}}{0.5\,\mathrm{k\Omega}} = 20\,\mathrm{mA}\ ;$$

Eq. [2.3] yields:

$$V_D = E\,\big|_{I_D=0\,\mathrm{A}} = 10\,\mathrm{V}\ ;$$

Example 2.1 Load-line Analysis Cont'd

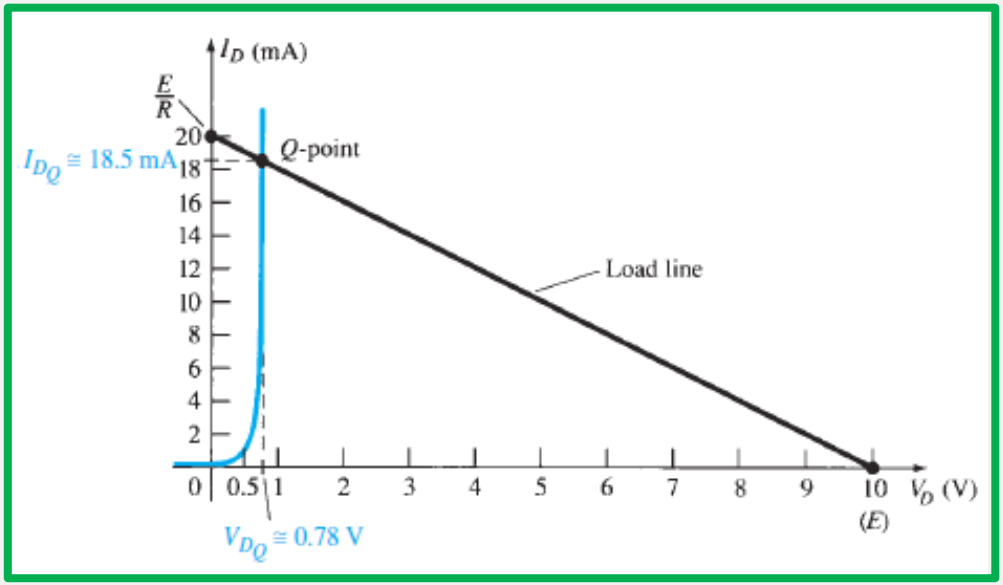


Figure 2.4: Solution to Example 2.1.

- The resultant load line appears in Fig. 2.4.
- The *Q*-point voltage and current are thus

$$V_{D_Q} \cong 0.78\text{V}$$

$$I_{D_Q} = 18.5\text{mA}$$

- The level of V_D is certainly an estimate, and the accuracy of I_D is limited by the chosen scale.
- A higher degree of accuracy would require a plot that would be much larger and perhaps unwieldly.

b) $V_R = E - V_D = 10\text{V} - 0.78\text{V}$; $\therefore \quad V_R = 9.22\text{V}$

2.1 Load-line Analysis Cont'd

- As noted in the example above, the load line is determined solely by the applied network, whereas the characteristics are defined by the chosen device.

- Since the network of Example 2.1 is a dc network the *Q*-point of Fig. 2.4 will remain fixed with $V_{D_Q} = 0.78\ \text{V}$ and $I_{D_Q} = 18.5\,\text{mA}$.
- Recall that we defined a dc resistance at any point on the characteristics by $R_{DC} = V_D / I_D$.
- Using the *Q*-point values, the dc resistance for Example 2.1 is thus

$$R_D = \frac{V_{D_Q}}{I_{D_Q}} = \frac{0.78\,\text{V}}{18.5\,\text{mA}} = 42.16\ \Omega$$

- Vividly once a dc *Q*-point has been determined the diode can be replaced by its dc resistance equivalent as shown in Fig. 2.5.

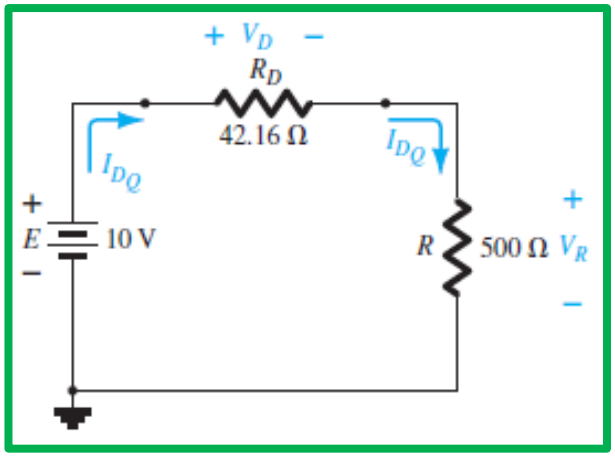


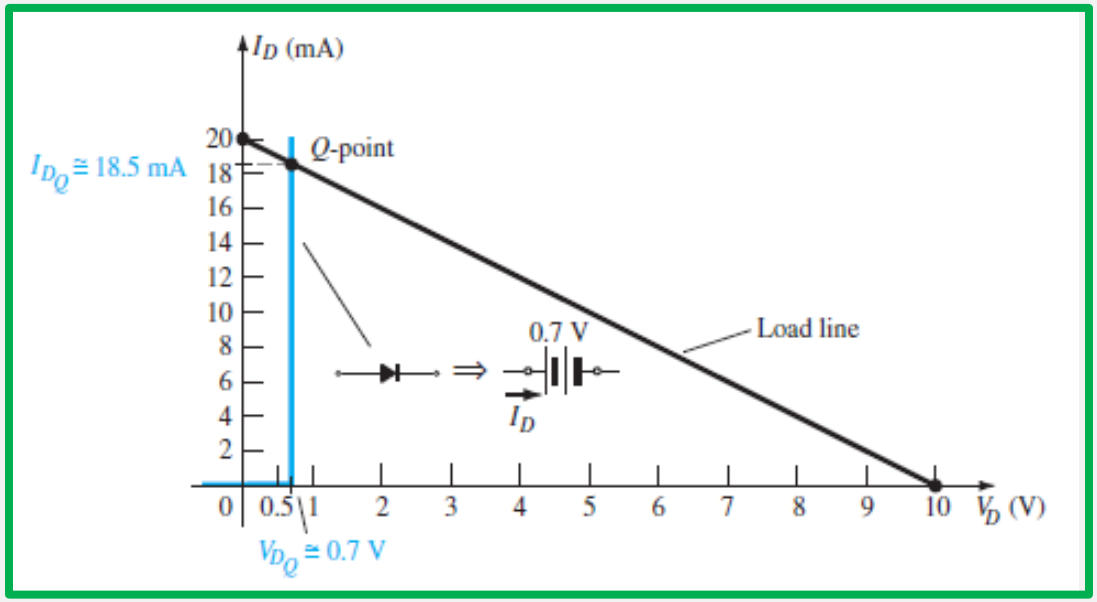
Figure 2.5: Network equivalent to Fig. 2.4

Example 2.2 Load-line Analysis

- Repeat Example 2.1 using the approximate equivalent model for the silicon semiconductor diode.

[Solution]

- The load line is redrawn as shown in Fig. 2.6 with the same intersection defined in Example 2.1. The characteristics for the approximate equivalent circuit for the diode have also been sketched on the same graph. The resulting *Q*-point is



$$V_{D_Q} = 0.7\text{V}$$

$$I_{D_Q} = 18.5\text{mA}$$

Figure 2.6: Soln to Example 2.1 using the diode approx. model

2.1 Load-line Analysis Cont'd

- Thus, for Example 2.2 the dc resistance of the *Q*-point is

$$R_D = \frac{V_{D_Q}}{I_{D_Q}} = \frac{0.7\,\text{V}}{18.5\,\text{mA}} = 37.84\ \Omega$$

- Notice that this value is relatively close to that obtained for full characteristics.

Example 2.3 Load-line Analysis

- Repeat Example 2.1 using the ideal diode model.

[Solution]

- As shown in Fig. 2.7, the load line is the same, but the ideal characteristics now intersect the load line on the vertical axis. The *Q*-point is therefor defined by

$V_{D_Q} = 0\,\text{V}$ $\quad$ $I_{D_Q} = 20\,\text{mA}$

Example 2.3 Load-line Analysis Cont'd

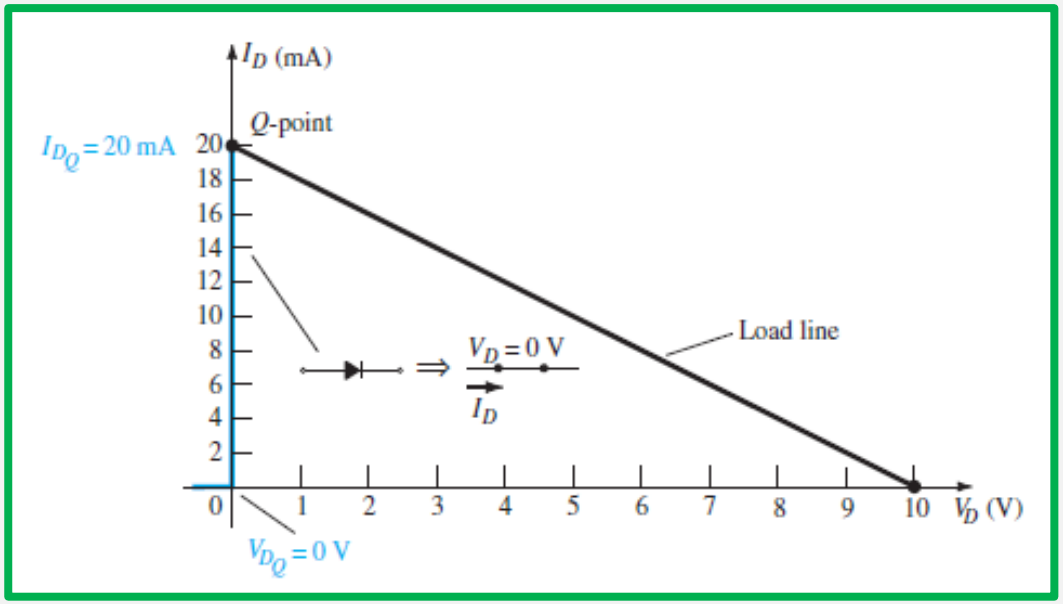


Figure 2.7: Solution to Example 2.1 using the ideal diode model.

- The results are sufficiently different from solutions of Example 2.1 to cause some concern about the accuracy.
- Thus, the approach of Example 2.2 is more appropriate compared to the ideal model.
- For Example 2.3 we have $R_D = \frac{V_{D_Q}}{I_{D_Q}} = \frac{0\,\text{V}}{20\,\text{mA}} = 0\,\Omega$

2.3 Series Diode Configurations

- The last section has shown that the approximate piecewise-linear equivalent model gives results quite close, if not equal, to the full characteristic model.
- Thus, for all analysis to follow in this lecture it is assumed that

- The forward resistance of a diode is usually so small compared to the other series elements of the network that it can be ignored.
- In general, a diode is in the "on" state if the current established by the applied sources is such that its direction matches that of the arrow in the diode symbol, and $V_D \geq 0.7\,\text{V}$ for silicon, $V_D \geq 0.3\,\text{V}$ for germanium, and $V_D \geq 1.2\,\text{V}$ for gallium arsenide.

Example 2.4 Series Diode Configuration

- For the series diode configuration of Fig. 2.8, determine V_D , V_R and I_D .

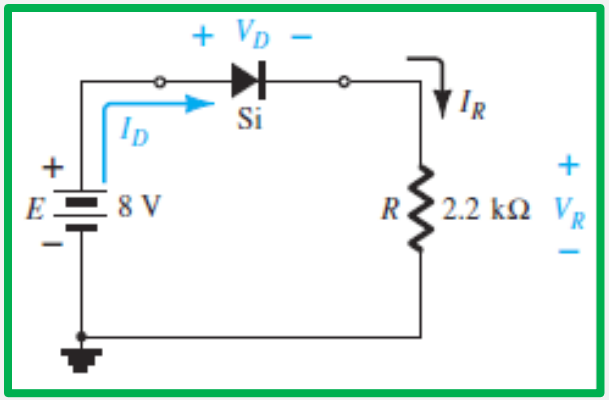


Figure 2.8: Circuit for Example 2.4.

[Solution]

- Since the applied voltage established a current in the clockwise direction to match the arrow of the symbol and the diode is in the "on" state,

$$V_D = 0.7\text{V}$$

$$V_R = E - V_D = 8\text{V} - 0.7\text{V}; \Rightarrow \quad V_R = 7.3\text{V}$$

$$I_D = I_R = \frac{V_R}{R} = \frac{7.3\text{V}}{2.2\,\text{k}\Omega}; \Rightarrow \quad I_D \cong 3.32\text{mA}$$

Example 2.5 Series Diode Configuration

- Repeat Example 2.4 with the diode reversed.

[Solution]

- The direction of the current is opposite to the arrow in the diode symbol and the diode equivalent is an open circuit no matter which model is employed.
- Applying Kirchhoff's voltage law to network of Fig. 2.9 yields,

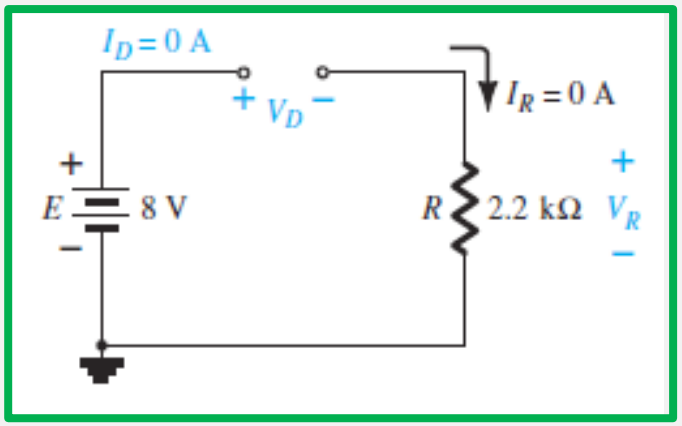


Figure 2.9: Determining unknown quantities for Example 2.5.

$$E - V_D - V_R = 0;$$

$$V_D = E - V_R = 8\text{V} - 0\text{V};$$

$$V_D = 8\text{V}$$

Example 2.6 Series Diode Configuration

- Determine V_o and I_D for the series circuit of Fig. 2.10.

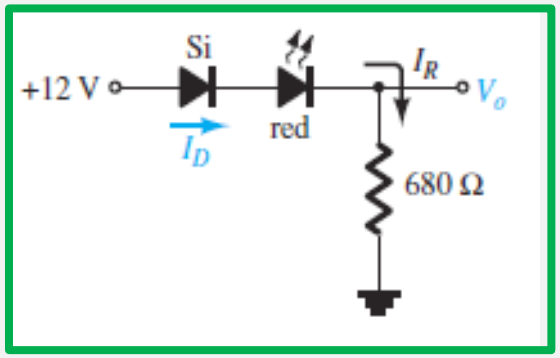


Figure 2.10: Circuit for Example 2.6.

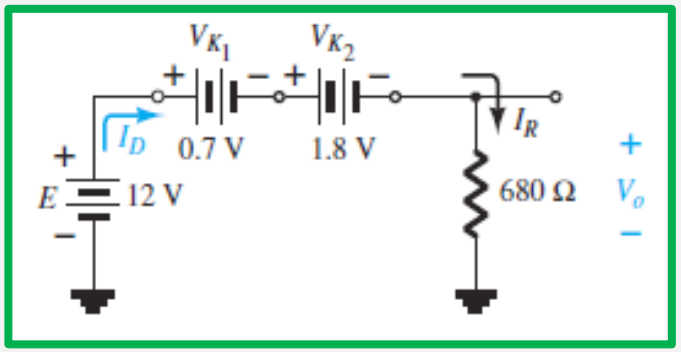


Figure 2.11: Determining unknown quantities for Example 2.6.

[Solution]

- Using the constant-voltage drop diode model, circuit is redrawn as shown in Fig. 2.11.
- Analysis of this ckt yields,

$$V_o = E - V_{K_1} - V_{K_2} = 12\,\text{V} - 2.5\,\text{V}; \Rightarrow$$

$$V_o = 9.5\,\text{V}$$

$$I_D = I_R = \frac{V_R}{R} = \frac{9.5\,\text{V}}{680\,\Omega}; \Rightarrow$$

$$I_D = 13.97\,\text{mA}$$

2.4 Parallel and Series-Parallel Diode Configurations

- The methods applied in section 2.4 can be extended to the analysis of parallel and series-parallel configurations.
- For each area of application, simply match the sequential series of steps applied to series diode configurations.

Example 2.7 Parallel and Series-Parallel Diode Configurations

- Determine the currents I_1 , I_2 , and I_{D_2} for the network of Fig. 2.12.

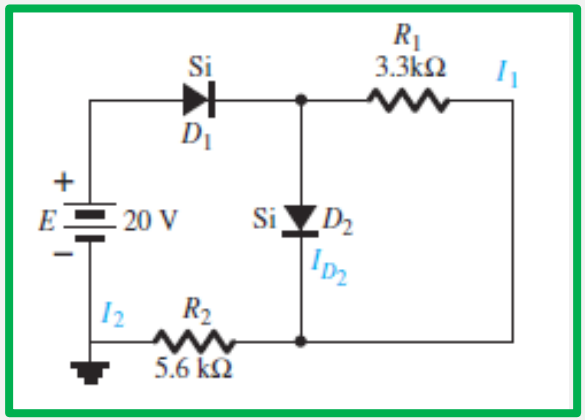


Figure 2.12: Circuit for Example 2.7.

[Solution]

- Clearly the flow of current will be such that both diodes will be in "on" state.
- Thus, the redrawn circuit is as shown in Fig. 2.13.

Example 2.7 Parallel and Series-Parallel Diode Configurations Cont'd

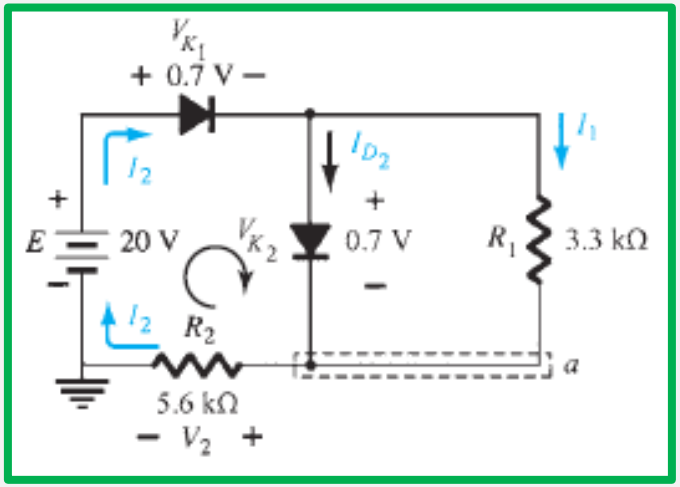


Figure 2.13: Determining unknown quantities for Example 2.7.

- Vividly,

$$I_1 = \frac{V_{K_2}}{R_1} = \frac{0.7\,\text{V}}{3.3\,\text{k}\Omega}\ ;\ \Rightarrow \quad \boxed{I_1 = 0.212\,\text{mA}}$$

- Applying KVL around the loop shown yields,

$$-V_2 + E - V_{K_1} - V_{K_2} = 0\,;$$

$$V_2 = E - V_{K_1} - V_{K_2} = 20\,\text{V} - 0.7\,\text{V} - 0.7\,\text{V}\,;$$

$$\boxed{V_2 = 18.6\,\text{V}}$$

- Thus,

$$\boxed{I_2 = 3.32\,\text{mA}}$$

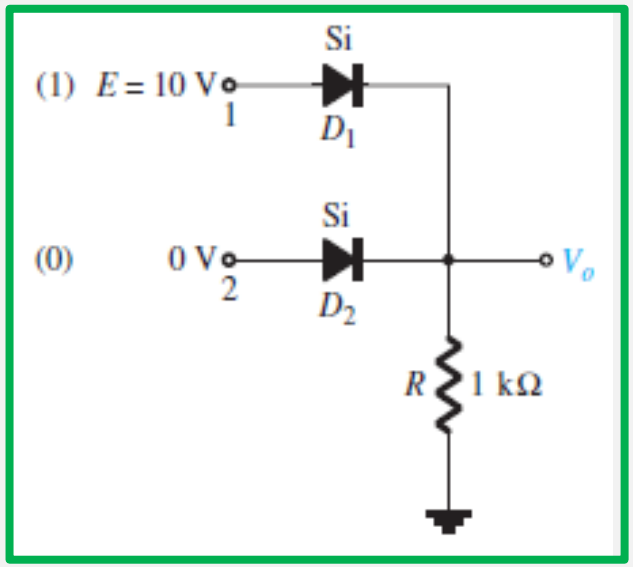
- At node a, $I_{D_2} + I_1 = I_2\ ;\quad \Rightarrow I_{D_2} = I_2 - I_1 = 3.32\,\text{mA} - 0.212\,\text{mA}\ ;$

$$\therefore\ \boxed{I_{D_2} \cong 3.11\,\text{mA}}$$

2.5 AND/OR Gates

- The analysis of AND/OR gates here is limited to determining the voltage levels and detailed discussion of Boolean algebra or positive and negative logic are left for the course EEE 3131.
- Thus, in the example that follows 10-V level is assigned a "logic 1" and 0- V input is assigned a "logic 0."

Example 2.8 AND/OR Gates



- Determine V_o for the network of Fig. 2.14.
- An OR gate is such that the output voltage level will be a 1 if either *or* both inputs is a 1. The output is a 0 if both inputs are at the 0 level.

Figure 2.14: Positive logic OR gate

Example 2.8 AND/OR Gates Cont'd

[Solution]

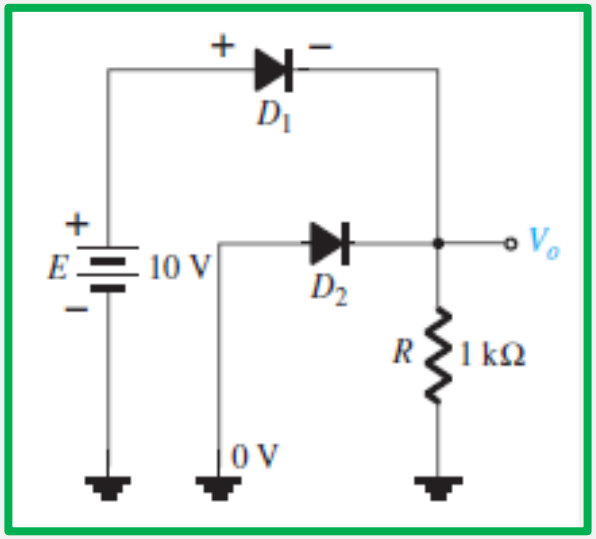


Figure 2.15: Redrawn network of Fig. 2.14.

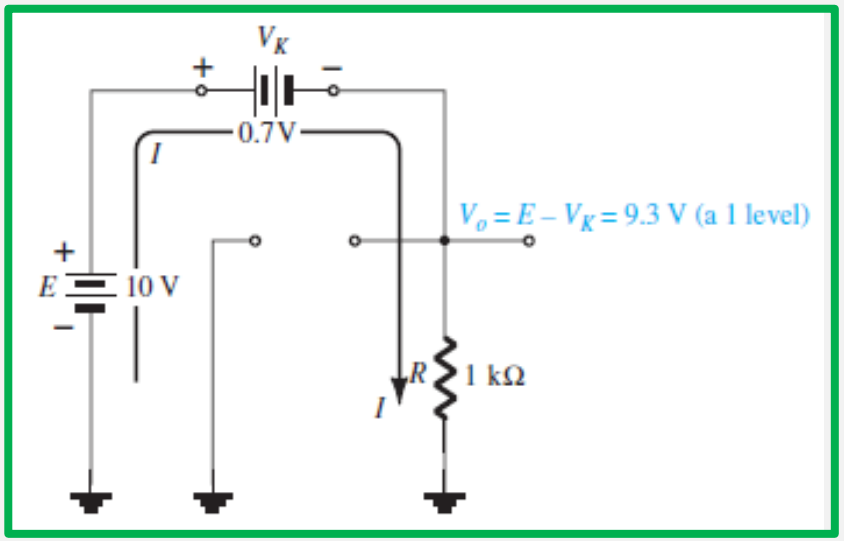


Figure 2.16: Assumed diode states for Fig. 2.40.

- Vividly, $V_o = E - V_D = 10\,\text{V} - 0.7\,\text{V}$; $\Rightarrow$ **$V_o = 9.3\,\text{V}$**
- Thus, $I_2 = \dfrac{E - V_D}{R} = \dfrac{10\,\text{V} - 0.7\,\text{V}}{1\,\text{k}\Omega}$; **$I = 9.3\,\text{mA}$**

Example 2.9 AND/OR Gates

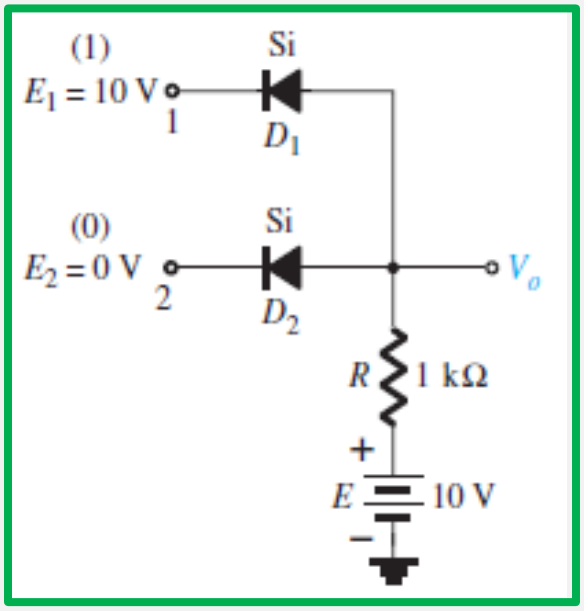


Figure 2.17: Positive logic AND gate.

- Determine the output level for the positive logic AND gate of Fig. 2.17. An AND gate is one where a 1 output is only obtained when a 1 input appears at each and every input.

[Solution]

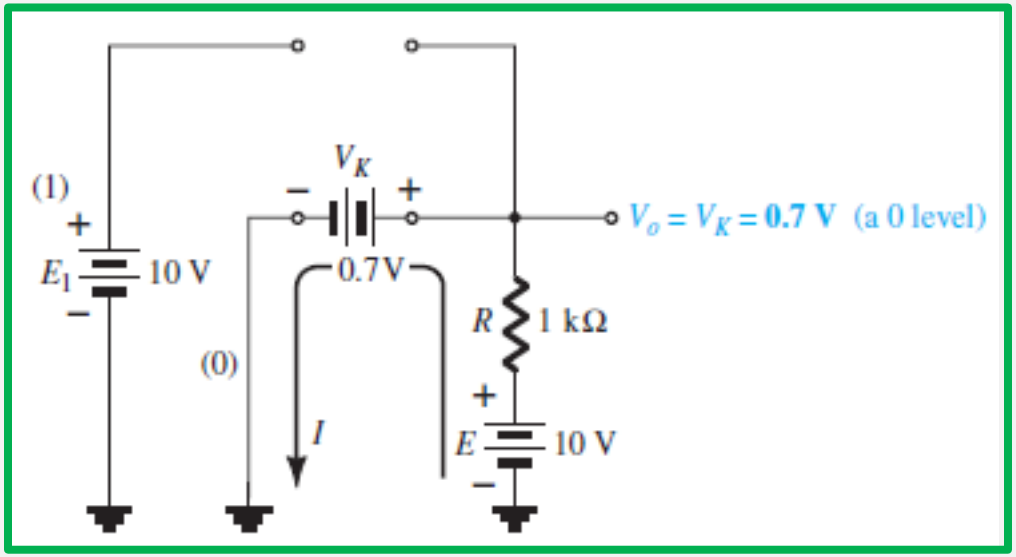


Figure 2.18: Assumed diode states for Fig. 2.17.

- Clearly, $V_o = 0.7\,\text{V}$

$$I_2 = \frac{E - V_K}{R} = \frac{10\,\text{V} - 0.7\,\text{V}}{1\,\text{k}\Omega}\ ; \qquad I = 9.3\ \text{mA}$$

2.6 Sinusoidal inputs; Half-Wave Rectification

- We now expand our diode analysis to include time-varying functions such as sinusoidal waveform and square wave.

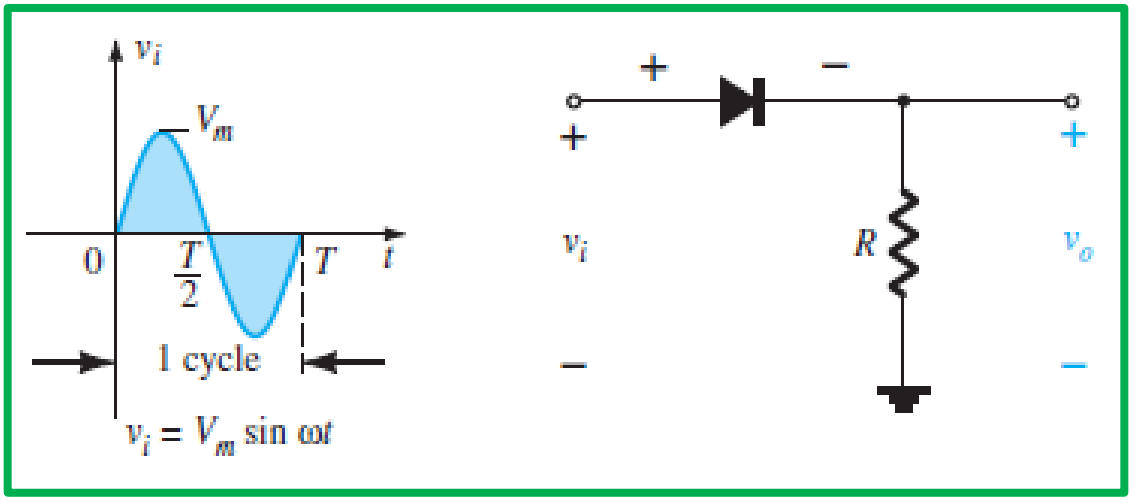


Figure 2.19: Half-wave rectifier.

- When employed in the rectification process, a diode is typically referred to as a rectifier.
- Its power and current ratings are typically much higher than diodes employed in other applications, such as computers and communication systems.

2.6 Sinusoidal inputs; Half-Wave Rectification Cont'd

- The effect of the positive and negative half cycles on the output are shown in the redrawn circuits below. Here an ideal diode is assumed.

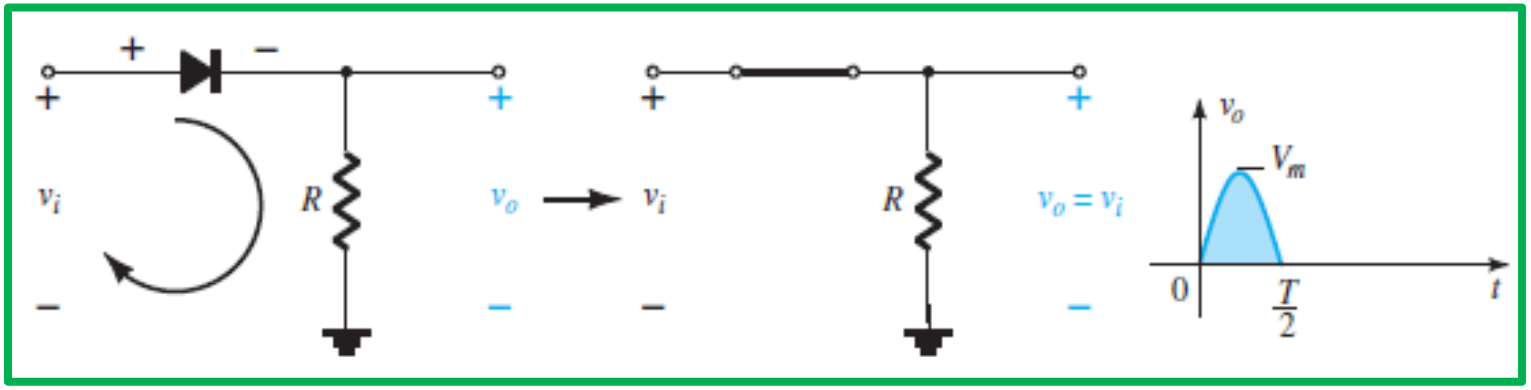


Figure 2.20: Conduction region $(0 \rightarrow T/2)$.

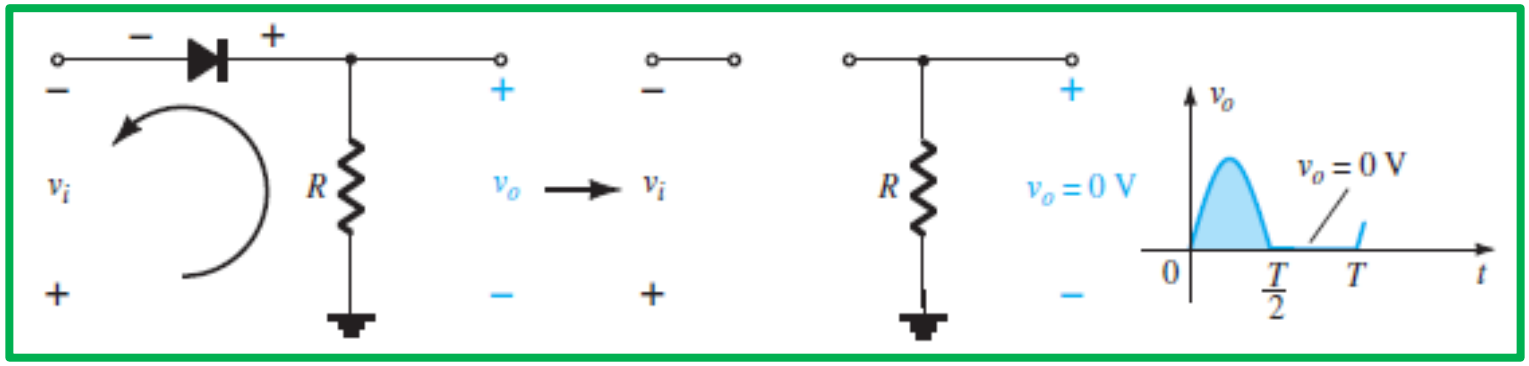


Figure 2.21: Nonconduction region $(T/2 \rightarrow T)$.

2.6 Sinusoidal inputs; Half-Wave Rectification Cont'd

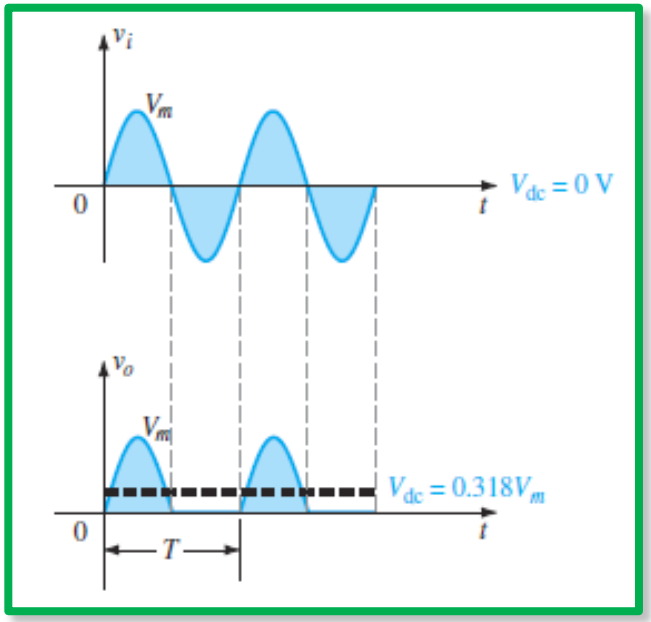


Figure 2.22: Half-wave rectified signal.

- The dc level for half-wave rectifier is obtained as follows:

$$V_{dc} = \frac{1}{T}\int_0^T v(t)\,dt = \frac{1}{T}\int_0^T V_m \sin \omega t\, dt\ ;$$

$$\Rightarrow \quad \boxed{V_{dc} = \frac{V_m}{\pi} = 0.318 V_m} \qquad \textbf{[2.5]}$$

- Fig. 2.23 demonstrates the effect of using a silicon diode with knee voltage $V_K = 0.7\,\text{V}$.

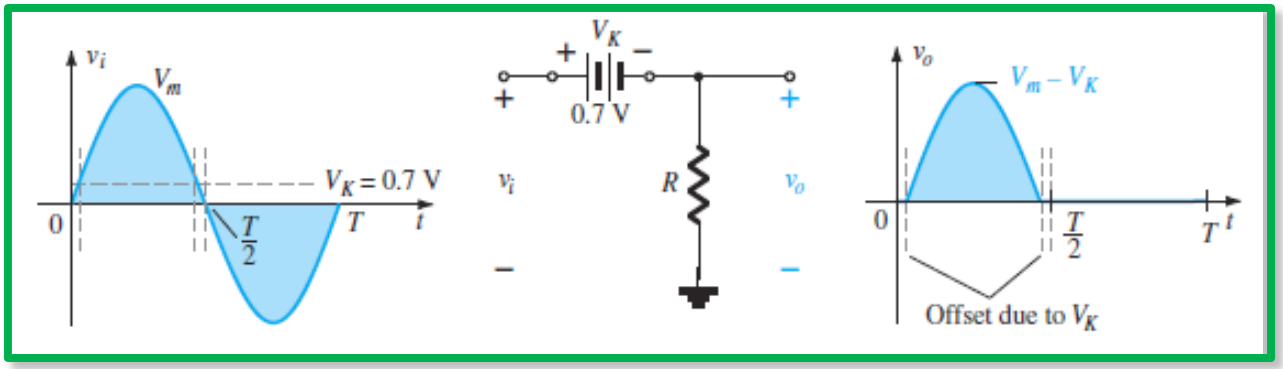


Figure 2.23: Effect of V_K on half-wave rectifier signal.

$$\therefore V_{dc} \cong 0.318\left(V_m - V_K\right)$$

[2.6]

2.6 Sinusoidal inputs; Half-Wave Rectification Cont'd

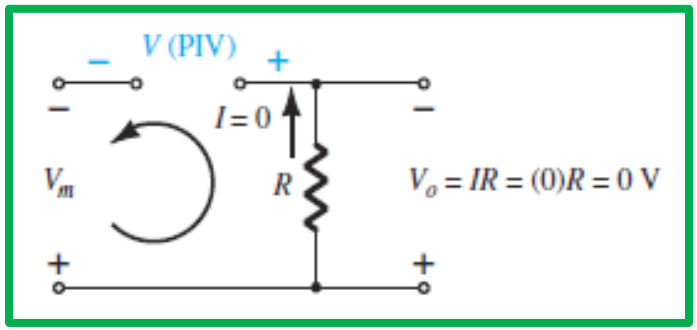


Figure 2.24: Determined the required PIV rating for the half-wave rectifier.

PIV (PRV)

- The peak inverse voltage (PIV) [or PRV (peak reverse voltage)] rating of the diode is critical in design of rectification systems.
- Recall that it is the voltage rating that must not be exceeded in the reverse-bias region or the diode will enter the Zener avalanche region.
- For a half-wave rectifier

$$\text{PIV rating} \geq V_m \qquad [2.7]$$

2.7 Full-Wave Rectification

Bridge Network

- The dc level obtained from a sinusoidal input can be improved 100% through full-wave rectification.

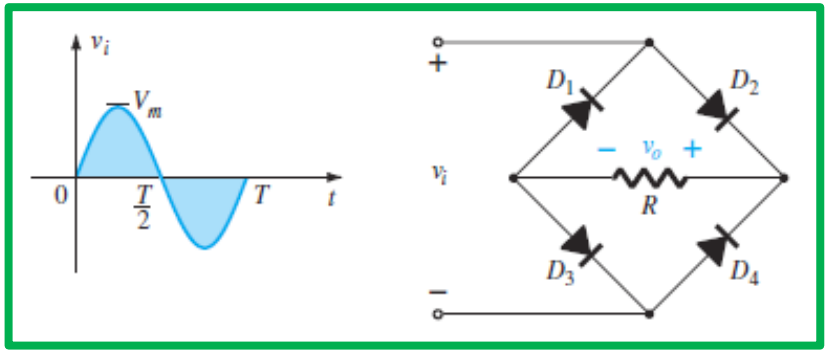


Figure 2.25: Full-wave bridge rectifier.

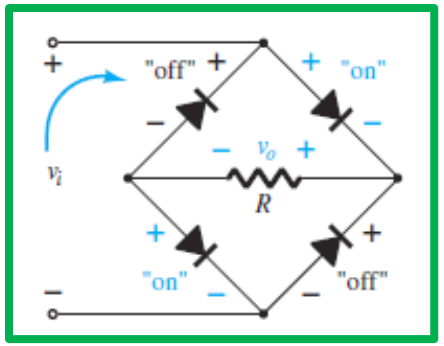


Figure 2.26: Network of Fig. 2.25 for half a period.

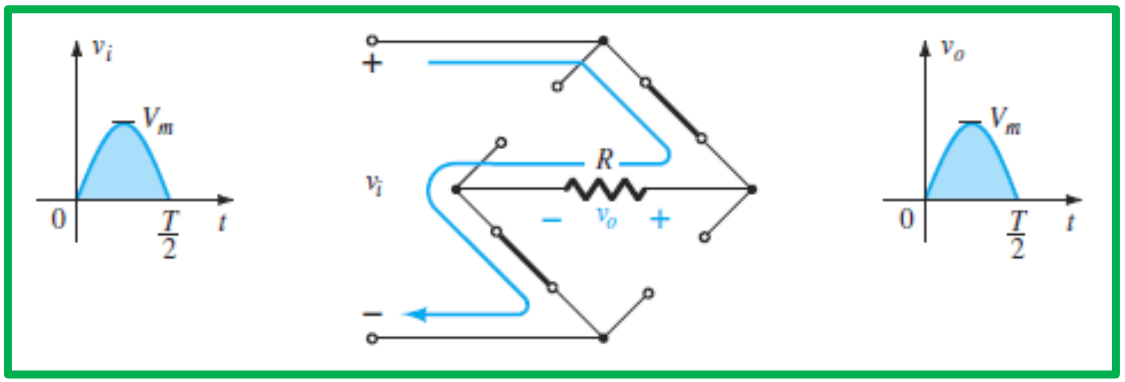


Figure 2.27: Conduction path for the positive region of v_i .

2.7 Full-Wave Rectification Cont'd

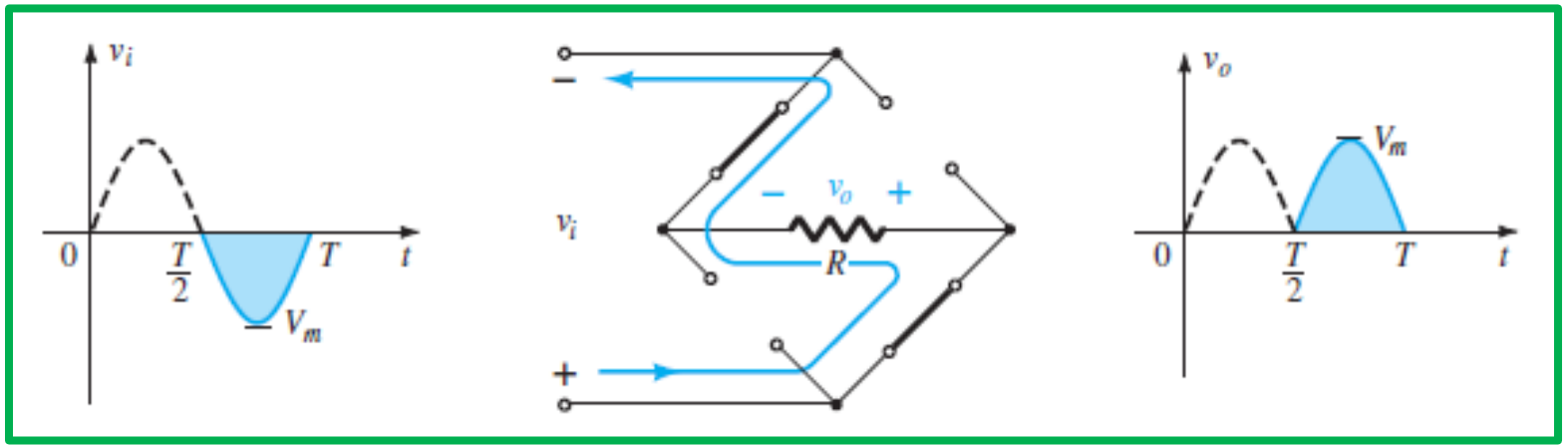


Figure 2.28: Conduction path for the negative region of v_i .

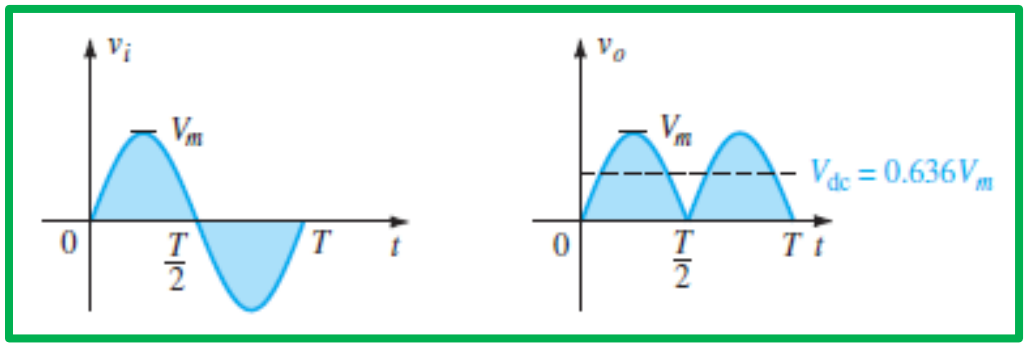


Figure 2.29: Input and output waveforms for a full-wave rectifier.

- For a full-wave rectifier we have,

$$V_{dc} = \frac{1}{T}\int_0^T \left|V_m \sin \omega t\right| dt \; ;$$

$$V_{dc} = \frac{2V_m}{\pi} = 0.636V_m \qquad [2.8]$$

2.7 Full-Wave Rectification Cont'd

- If silicon rather than ideal diodes are employed, applying KVL to the circuit of Fig. 2.30 yields,

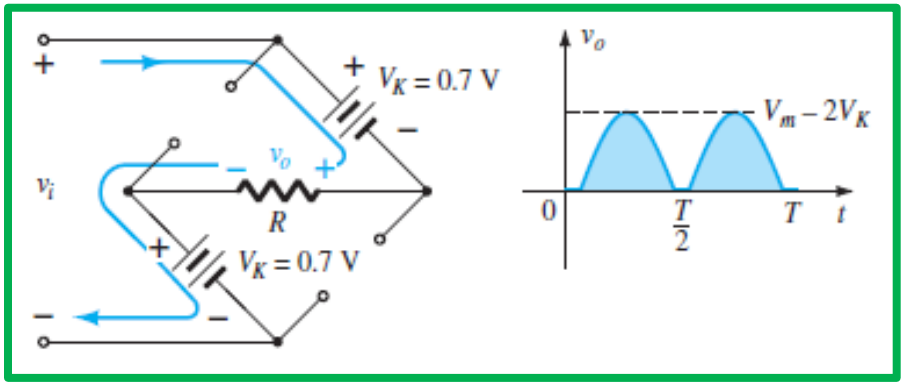


Figure 2.30: Determining $V_{o_{\max}}$ for Si diodes in the bridge configuration.

$$v_i - V_K - v_o - V_K = 0\,; \quad \Rightarrow \quad v_o = v_i - 2V_K$$

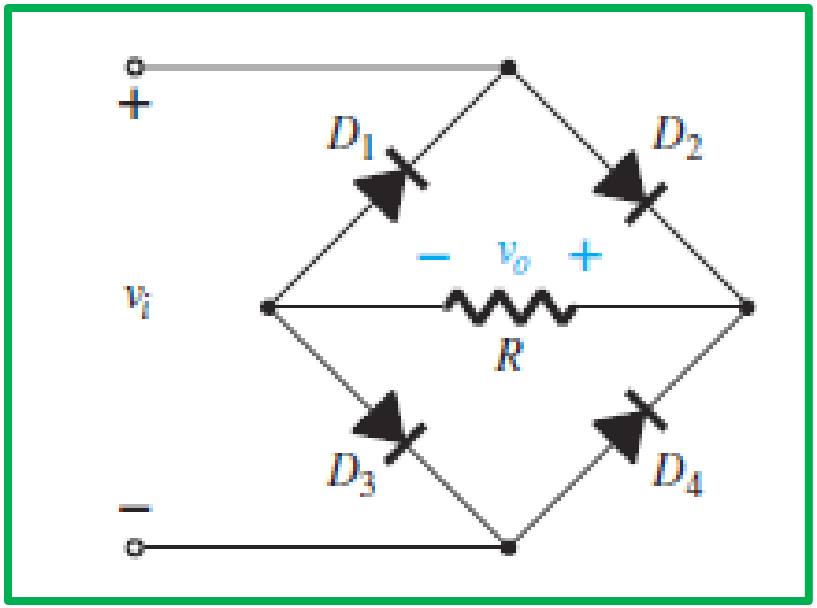
- Thus, the peak value of the output voltage is, $V_{o_{\max}} = V_m - 2V_K$
- For $V_m \gg 2V_K$, dc voltage is determined with relatively high level of accuracy using;

$$V_{dc} \cong \frac{2(V_m - 2V_K)}{\pi} = 0.636(V_m - 2V_K) \qquad [2.9]$$

2.7 Full-Wave Rectification Cont'd

- The **PIV** of each diode (ideal) in the full-wave rectifier is given by

$$\text{PIV rating} \geq V_m \qquad [2.10]$$



2.7 Full-Wave Rectification Cont'd

Center-Tapped Transformer

- The circuit configuration is given in Fig. 2.31.

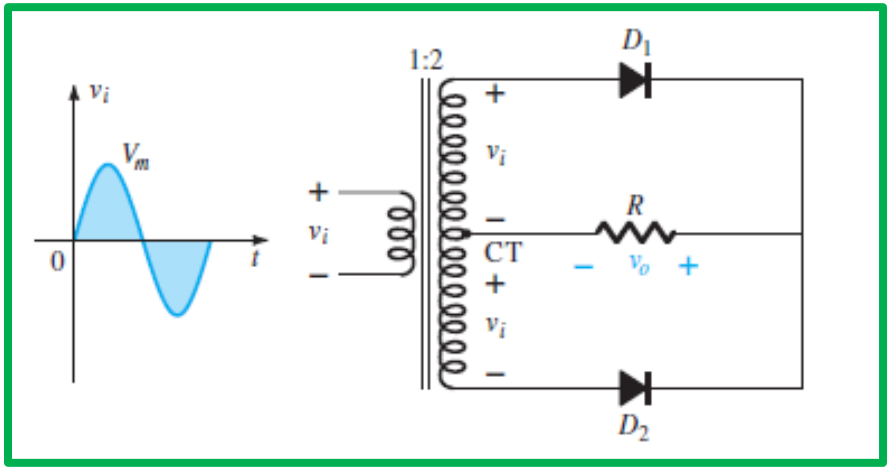


Figure 2.31: Center-tapped transformer full-wave rectifier.

2.7 Full-Wave Rectification Cont'd

- Analysis of center-tapped transformer full-wave rectifier.

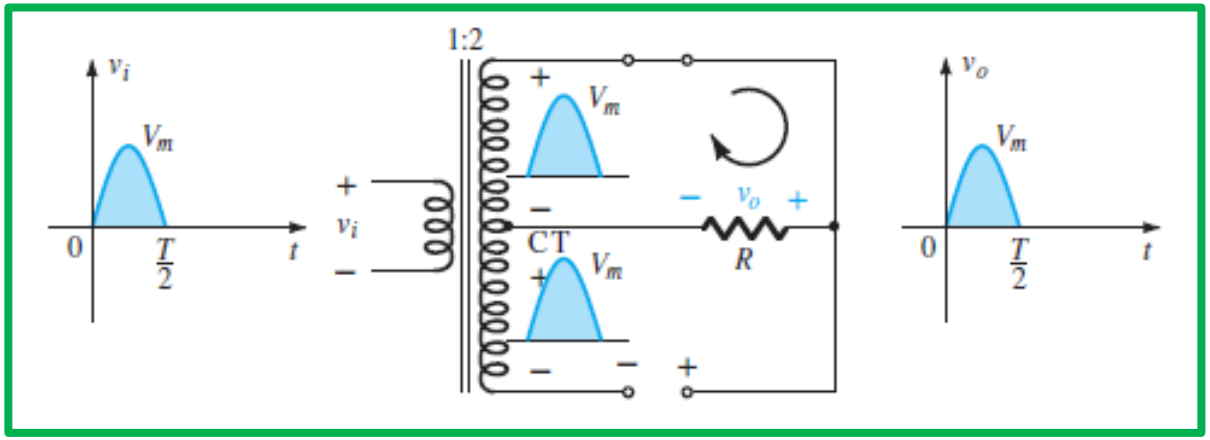


Figure 2.32: Network conditions for the positive region of v_i .

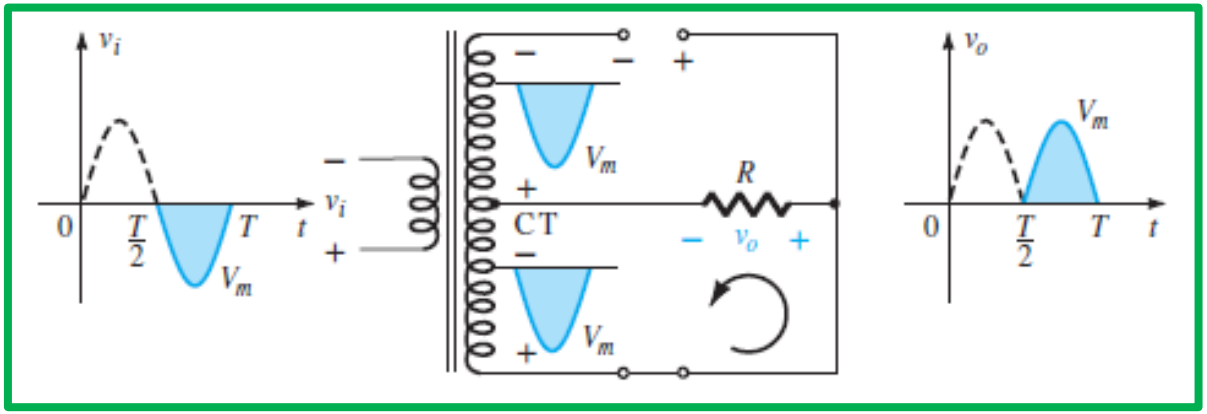
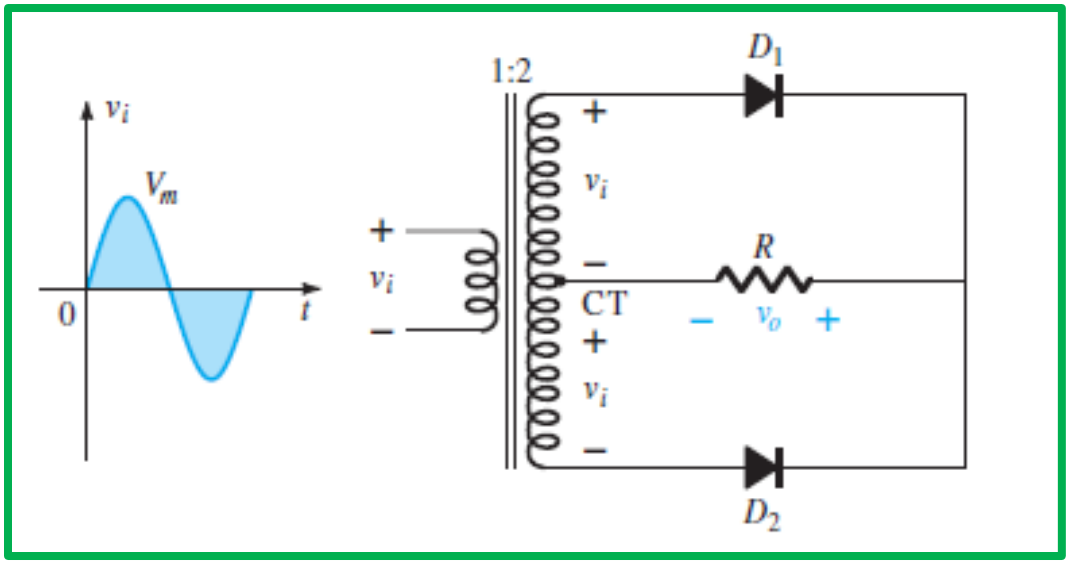


Figure 2.33: Network conditions for the negative region of v_i .

2.7 Full-Wave Rectification Cont'd

- **PIV.** The PIV for each diode in a CT transformer full-wave rectifier is thus,

$$\text{PIV rating} \geq 2V_m \qquad [2.11]$$



2.8 Clippers

- Clippers are networks that employ diodes to "clip" away a portion of an input signal without distorting the remaining part of the applied waveform.

Example 2.10 Series Clipper Circuit

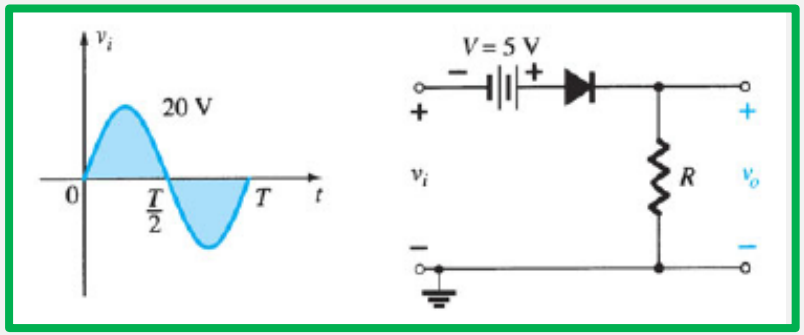


Figure 2.34: Series clipper for Example 2.10.

- Determine the output waveform for the sinusoidal input of Fig. 2.34.

[Solution]

Example 2.10 Series Clipper Circuit Cont'd

- ***Step 1***: The output is directly across the resistor *R*.
- ***Step 2***: Both v_i and dc supply are applying "pressure" to turn the diode on.
- ***Step 3***: The transition model is substituted as shown in Fig. 2.35. Thus, transition from one state to the other will occur when,

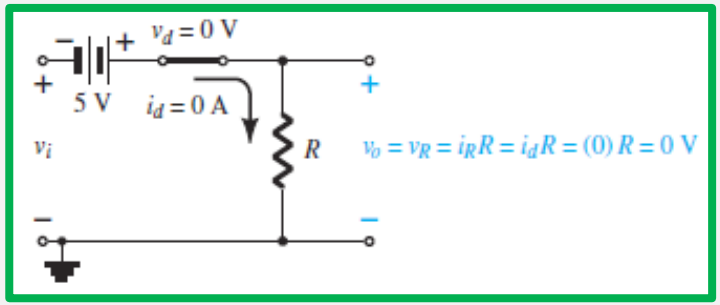


Figure 2.35: Determining transition level for the clipper of Fig. 2.35.

$$v_i + 5\,\text{V} = 0\,\text{V}\ ;\ \Rightarrow \quad \boxed{v_i = -5\,\text{V}}$$

- ***Step 4***: In Fig. 2.36 a horizontal line is drawn through the applied voltage at the transition level.
- Clearly, the diode is open-circuit for all $v_i < -5$ V and output is 0 V. For all $v_i > -5$ V short-circuit and the output $v_o = v_i + 5\,\text{V}$.

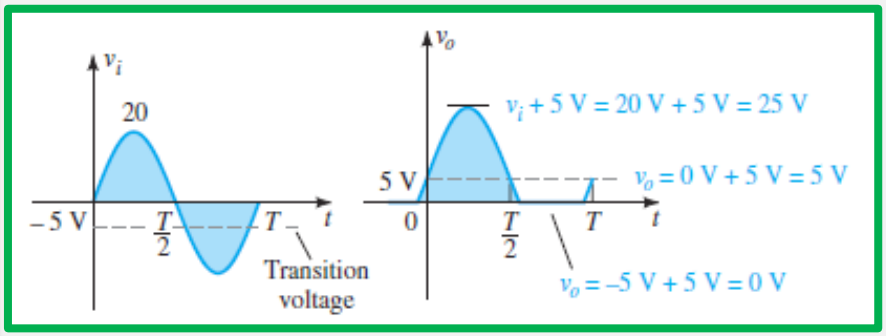


Figure 2.36: Sketch of the output voltage.

Example 2.11 Parallel Clipper Circuit

- Determine v_o for the network of Fig. 2.37. Assume a silicon diode, $V_K = 0.7\,\text{V}$.

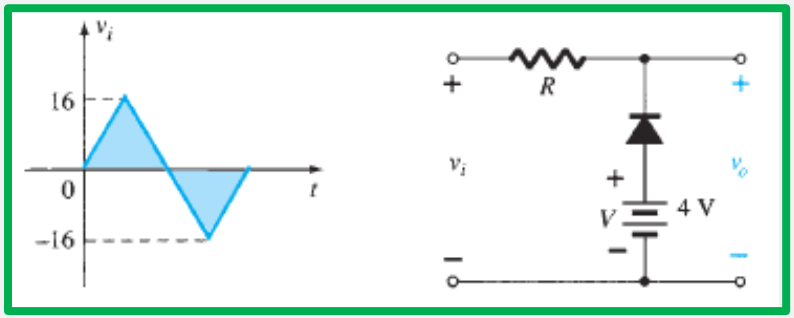


Figure 2.37: Example 2.11.

[Solution]

- The transition voltage is determined by letting, $i_d = 0\,\text{A}$ at $v_d = V_K = 0.7\,\text{V}$ and obtaining Fig. 2.38. Thus, KVL yields

$$v_i + V_K - V = 0\,;$$

$$v_i = V - V_K = 4\,\text{V} - 0.7\,\text{V} = \mathbf{3.3\,V}$$

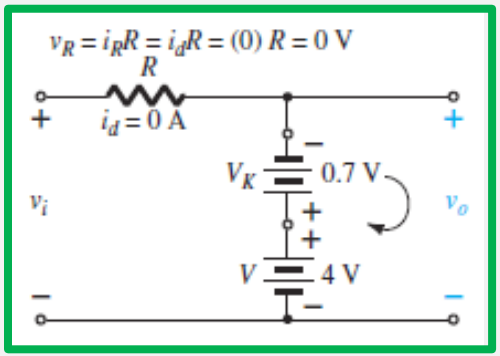


Figure 2.38: Sketch of to determine transition voltage.

- Thus, for all $v_i > 3.3\,\text{V}$, the diode is open-circuit and $v_o = v_i$. For all $v_i < 3.3\,\text{V}$ the diode is "on" and we have $v_o = 4\,\text{V} - 0.7\,\text{V} = \mathbf{3.3\,V}$.

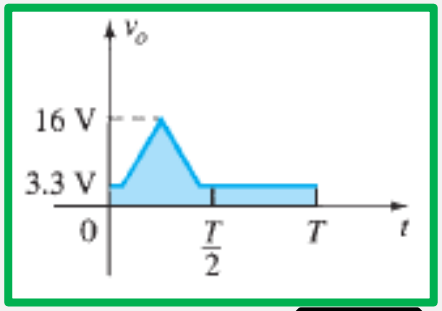


Figure 2.39: Sketch of the output voltage.

2.9 Clampers

- A clamper is a network constructed of a diode, a resistor, and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal.

Example 2.12 Clampers

- Determine v_o for the network of Fig. 2.40 having a Si diode with $V_K = 0.7\,\text{V}$.

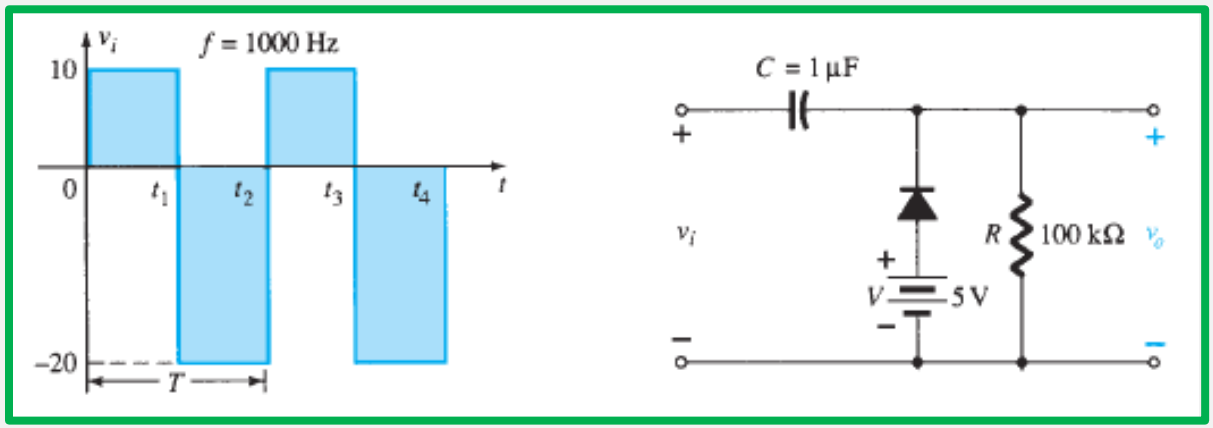
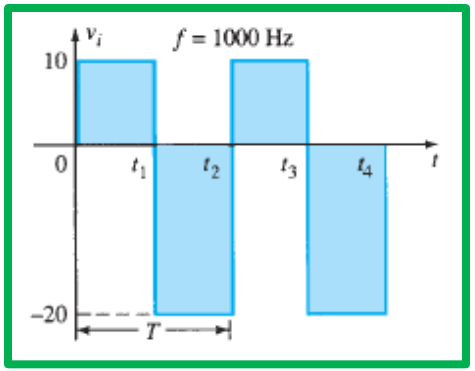


Figure 2.40: Applied signal and network for Example 2.12.

Example 2.12 Clampers Cont'd



[Solution]

- Note that the frequency is 1000 Hz, resulting in a period of 1 ms and an interval of 0.5 ms between levels.
- The analysis begins with the interval $t_1 \rightarrow t_2$ of the input signal since the diode is in short-circuit state, resulting in Fig. 2.41.

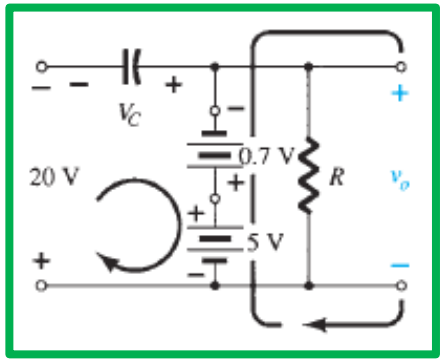


Figure 2.41:
Determining v_o and V with diode in the "on" state.

- KVL applied to the output section yields,

$$5\text{V} - 0.7\text{ V} - v_o = 0\,; \Rightarrow v_o = 5\text{V} - 0.7\text{ V} = \mathbf{4.3\,V}$$

- For the input section applying KVL yields,

$$-20\text{V} + V_C + 0.7\text{ V} - 5\text{ V} = 0\,;$$

$$\Rightarrow V_C = 25\text{V} - 0.7\text{ V} = \mathbf{24.3\,V}$$

Example 2.12 Clampers Cont'd

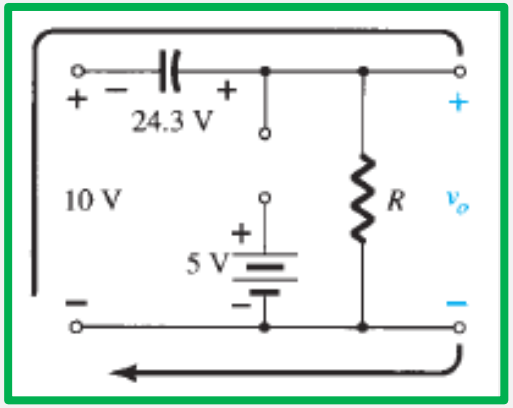


Figure 2.42: Determining v_o diode in open state.

- Tor the interval $t_2 \rightarrow t_3$ the network will now appear as in Fig. 2.42, with the only change being the voltage across the capacitor.
- Applying Kirchhoff's voltage law yields

$$+10\,\text{V} + 24.3\,\text{V} - v_o = 0\,; \qquad \Rightarrow \; v_o = \mathbf{34.3\,V}$$

- The resultant waveform is shown in Fig. 2.43.

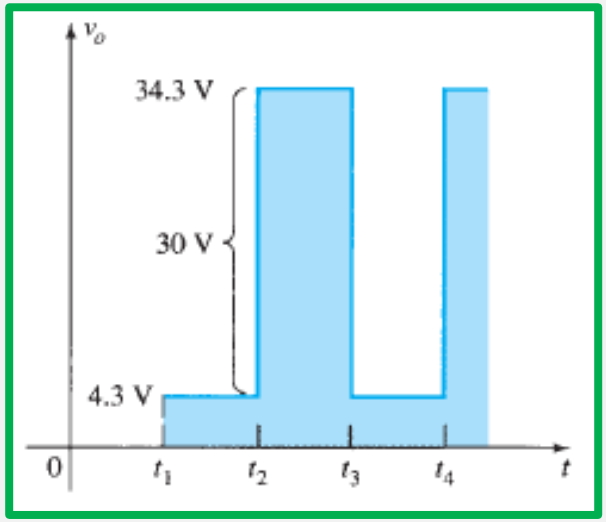


Figure 2.43: Sketch for clamper of Fig. 2.40.

2.10 Networks With a DC and AC Source

- The response of any network with both an ac and dc source can be found by finding the response to each source independently and then combining the results.

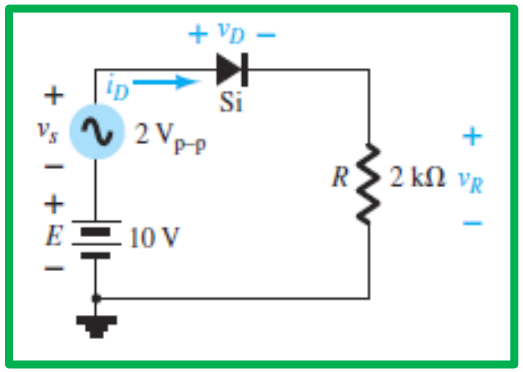


Figure 2.44: Network with a dc and ac supply.

DC Source

- Consider the circuit of Fig. 2.44. The network is redrawn with in Fig. 2.45 with dc source only.
- Using the approximate equivalent circuit for the diode, the output voltage is thus,

$$V_R = E - V_D = 10\text{V} - 0.7\text{V} = \mathbf{9.3\,V};$$

$$I_D = I_R = \frac{9.3\text{V}}{2\text{k}\Omega} = \mathbf{4.65\,mA}$$

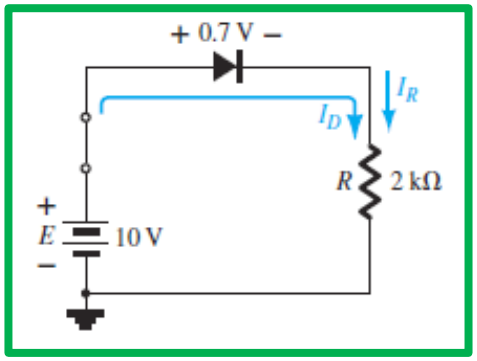


Figure 2.45: Applying superposition to determine effects of dc source.

2.10 Networks With a DC and AC Source Cont'd

AC Source

- The dc source is also replaced by a short-circuit, see Fig. 2.46. Then the diode is replaced by the ac resistance as determined in lecture 1, see Fig. 2.47.
- In this case, $r_d = \frac{26\,\text{mV}}{I_D} = \frac{26\,\text{mV}}{4.65\,\text{mA}} = \mathbf{5.59\,\Omega}$

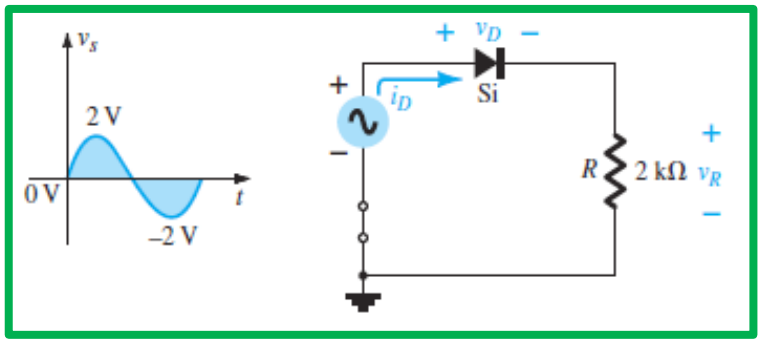


Figure 2.46: Determining effects of ac source on output.

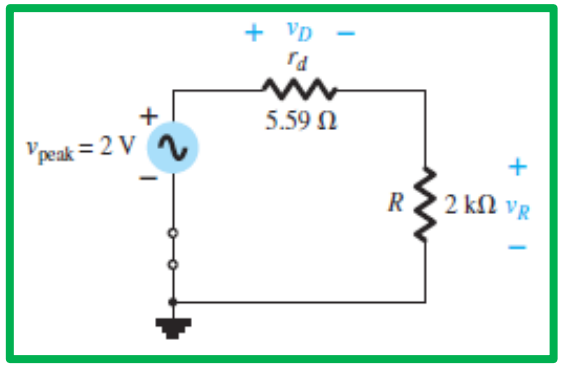


Figure 2.47: Diode replaced by its ac equivalent resistance.

- The peak values are thus,

$$v_{R_{peak}} = \frac{(2\text{k}\Omega)(2\text{V})}{2\text{k}\Omega + 5.59\,\Omega} \cong \mathbf{1.99\,V}\ ; \qquad v_{D_{peak}} = v_{s_{peak}} - v_{R_{peak}} = 2\text{V} - 1.99V = \mathbf{10\,mV}$$

2.10 Networks With a DC and AC Source Cont'd

- Superposition of dc and ac analysis results yields the waveform in Fig. 2.48.

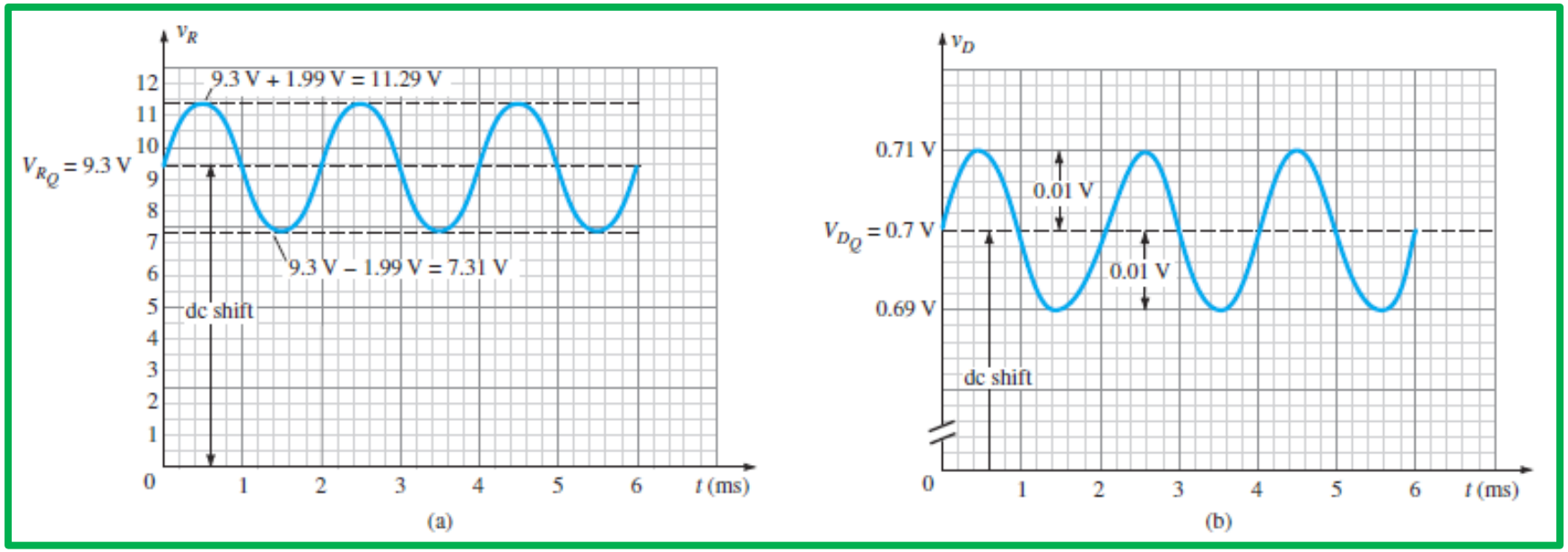


Figure 2.48: (a) v_R and (b) v_D for the network of Fig. 2.44.

- Note that the diode has an important impact on the resulting output voltage v_R but very little impact on the ac swing..

2.10 Networks With a DC and AC Source Cont'd

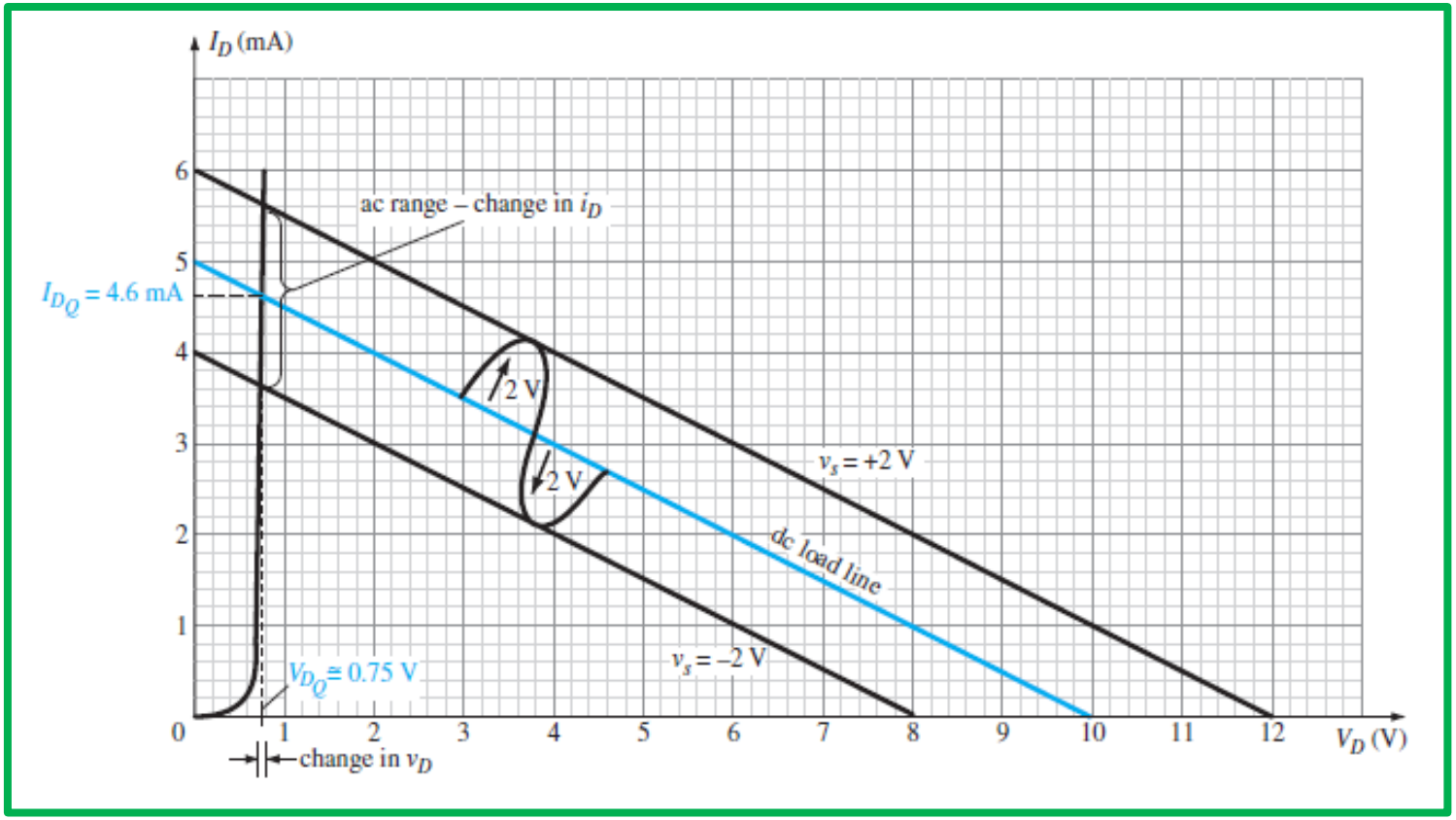


Figure 2.49: Shifting load line due to v_s source.

- In Fig. 2.49 the dc load line has been drawn as described in section 2.2. The actual characteristics and load-line are used to find the *Q*-point.

2.10 Networks With a DC and AC Source Cont'd

- For the peak value of input voltage the load line will have voltage and current axes intercepts respectively at

$$E = \mathbf{12\,V} \quad \text{and} \quad I = \frac{E}{R} = \frac{12\,\text{V}}{2\,\text{k}\Omega} = \mathbf{6\,mA}$$

- Similarly, the negative peak intercepts are at $E = \mathbf{8V}$ and $I = \mathbf{4\,mA}$.
- The Quiescent value of dc current is $I_{D_Q} \cong \mathbf{4.6\,mA}$, the ac resistance is thus,

$$r_d = \frac{26\,\text{mV}}{I_{D_Q}} = \frac{26\,\text{mV}}{4.6\,\text{mA}} = \mathbf{5.65\,\Omega}$$

- This value is very close to the value we found earlier using the approximate equivalent circuit.

2.12 AM Signal Demodulation

- Another common use of diodes is rectification called demodulation or detection of modulated signals such as those used for radio frequency broadcasting and other radio communication systems.
- The demodulator in Fig. 2.55 works in a similar manner to the half-wave rectifier described earlier.
- When the HF modulated signal passes through a diode only the positive half each cycle is applied to the low-pass filter formed by R_1 and C_1.
  - Thus, the carrier is removed, leaving only the required LF signal plus a dc component.
  - The high-pass filter formed by R_2 and C_2 removes the dc component.

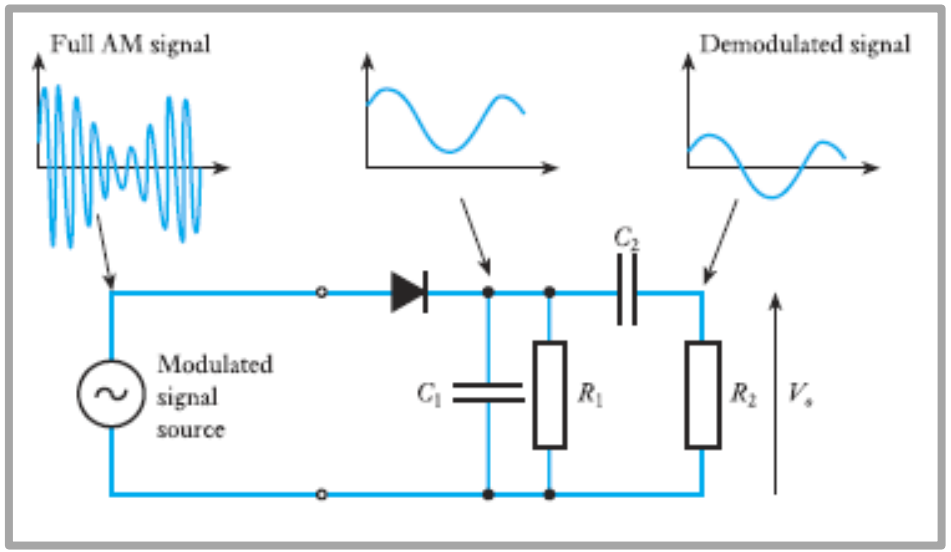


Figure 2.55: AM Signal Demodulator.

2.11 Zener Diodes Cont'd

- The analysis of networks employing Zener diodes is quite similar to that of semiconductor diodes seen earlier.
- A Zener diode assuming the straight-line approximation is shown in Fig. 2.50.

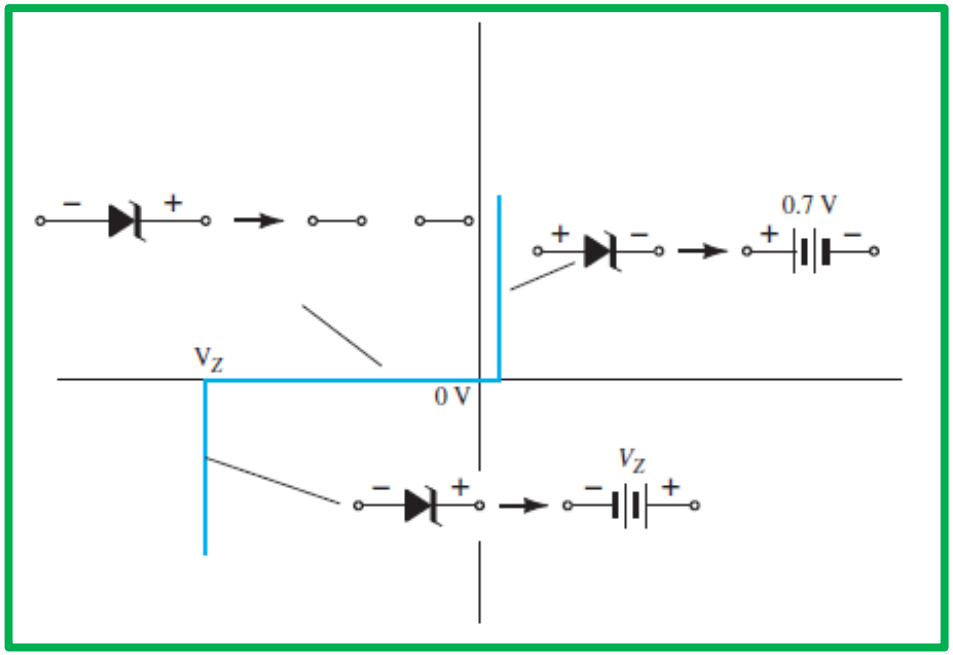


Figure 2.50: Approximate equivalent circuits for the Zener diode in the three possible regions.

2.11 Zener Diodes

- The use of the Zener diode as a regulator is so common. Let us analyse the basic configuration in Fig. 2.51.
- We consider *first fixed quantities*, followed by a *fixed supply voltage* and a *variable load*, and finally a *fixed load and a variable supply*.

V_i and R Fixed

- **Step 1**: Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit, see Fig. 2.52.

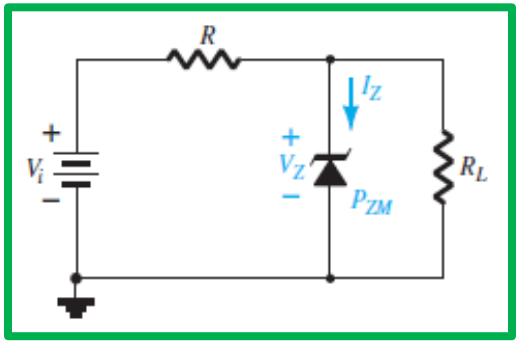


Figure 2.51: Basic Zener regulator.

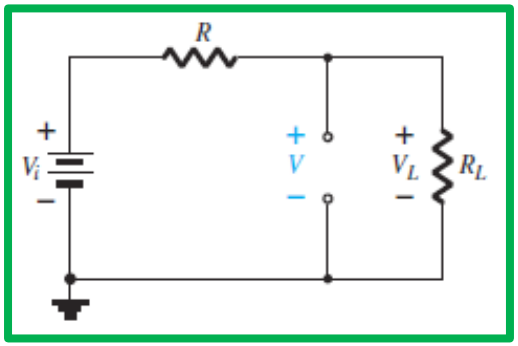


Figure 2.52: Determining the state of Zener diode.

- Voltage divider applied to Fig. 2.52 yields,

$$V = V_L = \frac{R_L}{R + R_L} V_i \qquad [2.12]$$

2.11 Zener Diodes Cont'd

- If $V \geq V_Z$, the Zener diode is on, and the appropriate equivalent model can be substituted.
- If $V < V_Z$, the diode is off, and the open-circuit equivalent is substituted.
- **Step 2**: Substitute the appropriate equivalent circuit and solve for the desired unknowns.
- For the circuit of Fig. 2.51 the "on" state yields Fig. 2.53.
- Vividly, $V_L = V_Z$ **[2.13]**

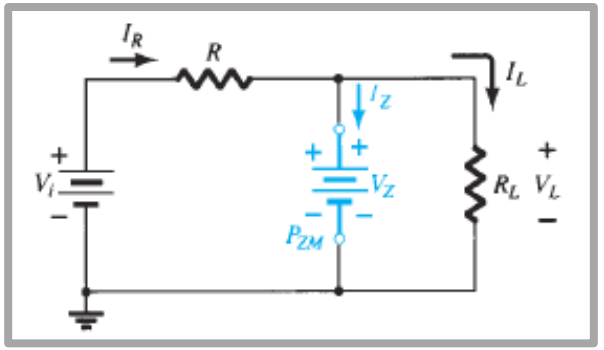


Figure 2.53: Basic Zener regulator.

- The Zener diode current is determined by exploiting Kirchhoff's current law (KCL),

$$I_R = I_Z + I_L \; ; \qquad I_Z = I_R - I_L \qquad \textbf{[2.14]}$$

where, $I_L = \dfrac{V_L}{R_L}$; and $I_R = \dfrac{V_R}{R} = \dfrac{V_i - V_L}{R}$;

2.11 Zener Diodes Cont'd

- Power dissipated by the Zener diode is $P_Z = V_Z I_Z$ [2.15]

- The dissipated power, P_Z ought to be less than the rated power, P_{ZM} for the device .

2.11 Zener Diodes Cont'd

Fixed V_i, Variable R_L

- Due to the offset voltage V_Z, there is a specific range of resistor values that will ensure that the Zener is in "on" state.
- To determine the minimum load resistance of Fig. 2.51 that will turn the Zener diode on, simply calculate the value of R_L, that will result in a load voltage $V_L = V_Z$. That is,

$$V_L = V_Z = \frac{R_L}{R_L + R} V_i \; ; \; \Rightarrow \; \boxed{R_{L,\min} = \frac{R}{V_i - V_Z} V_Z} \qquad [2.16]$$

- The condition defined by Eq. [2.16] in turn specifies the minimum I_L as

$$\boxed{I_{L,\min} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L,\min}}} \qquad [2.17]$$

2.11 Zener Diodes Cont'd

Fixed R_L, Variable V_i

- For fixed values of R_L in Fig. 2.51, the voltage V_i must be sufficiently large to turn the Zener diode on. The minimum turn-on voltage is

$$V_L = V_Z = \frac{R_L}{R_L + R} V_i \; ; \; \Rightarrow \quad \boxed{V_{i,\min} = \left(\frac{R_L + R}{R_L} \right) V_Z} \qquad [2.23]$$

- The maximum value of V_i is limited by the maximum Zener current I_{ZM} i.e.,

$$I_{ZM} = I_R - I_L \; ; \; \Rightarrow \quad \boxed{I_{R,\max} = I_{ZM} + I_L} \qquad [2.24]$$

- Since I_L is fixed at V_Z / R_L and I_{ZM} is the maximum value of I_Z, the maximum V_i is defined by

$$V_{i,\max} = V_{R,\max} + V_Z \; ; \; \Rightarrow \quad \boxed{V_{i,\max} = R I_{R,\max} + V_Z} \qquad [2.25]$$

Example 2.13 Zener Diodes

- Determine the range of values of V_i that will maintain the Zener diode of Fig. 2.54 in the "on" state.

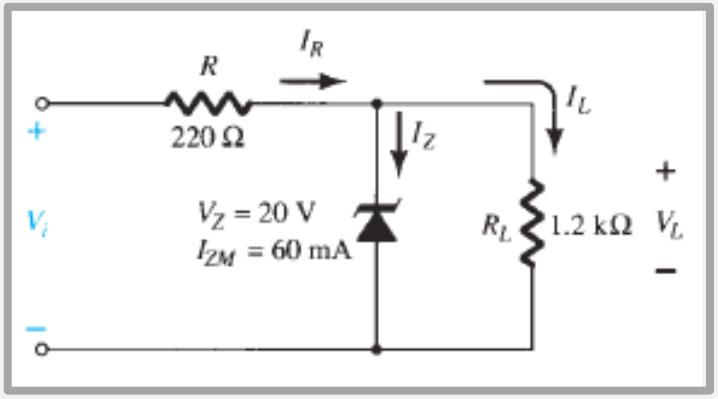


Figure 2.54: Zener Regulator for Example 2.13.

[Solution]

- Eq. [2.23]:

$$V_{i,\min} = \left(\frac{R_L + R}{R_L}\right)V_Z = \left(\frac{1200\Omega + 220\Omega}{1200\Omega}\right)(20\,\text{V});$$

$$\boxed{V_{i,\min} = 23.67\,\text{V}}$$

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{20\,\text{V}}{1200\Omega};$$

$$\boxed{I_L = 16.67\,\text{mA}}$$

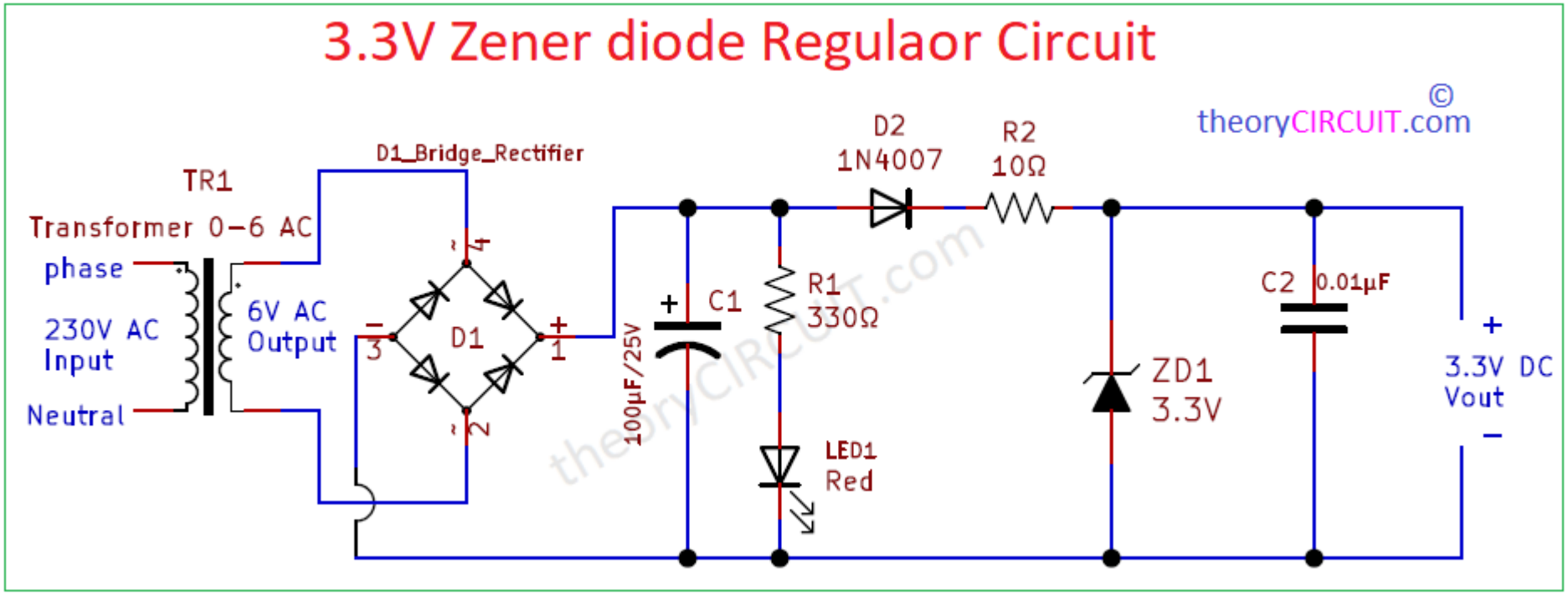
- Eq. [2.24]: $I_{R,\max} = I_{ZM} + I_L = 60\,\text{mA} + 16.67\,\text{mA};$ $\boxed{I_{R,\max} = 76.67\,\text{mA}}$

- Eq. [2.23]: $V_{i,\max} = RI_{R,\max} + V_Z = (0.22\,\text{k}\Omega)(76.67\,\text{mA}) + 20\,\text{V} = 16.87\,\text{V} + 20\,\text{V};$

$$\boxed{V_{i,\max} = 36.87\,\text{V}}$$

- Thus $\boxed{23.67 \le V_i \le 36.87\,\text{V}}$

Example CCT using Zener Diode



End of Lecture 2