EEE 3571 Electronic Engineering I

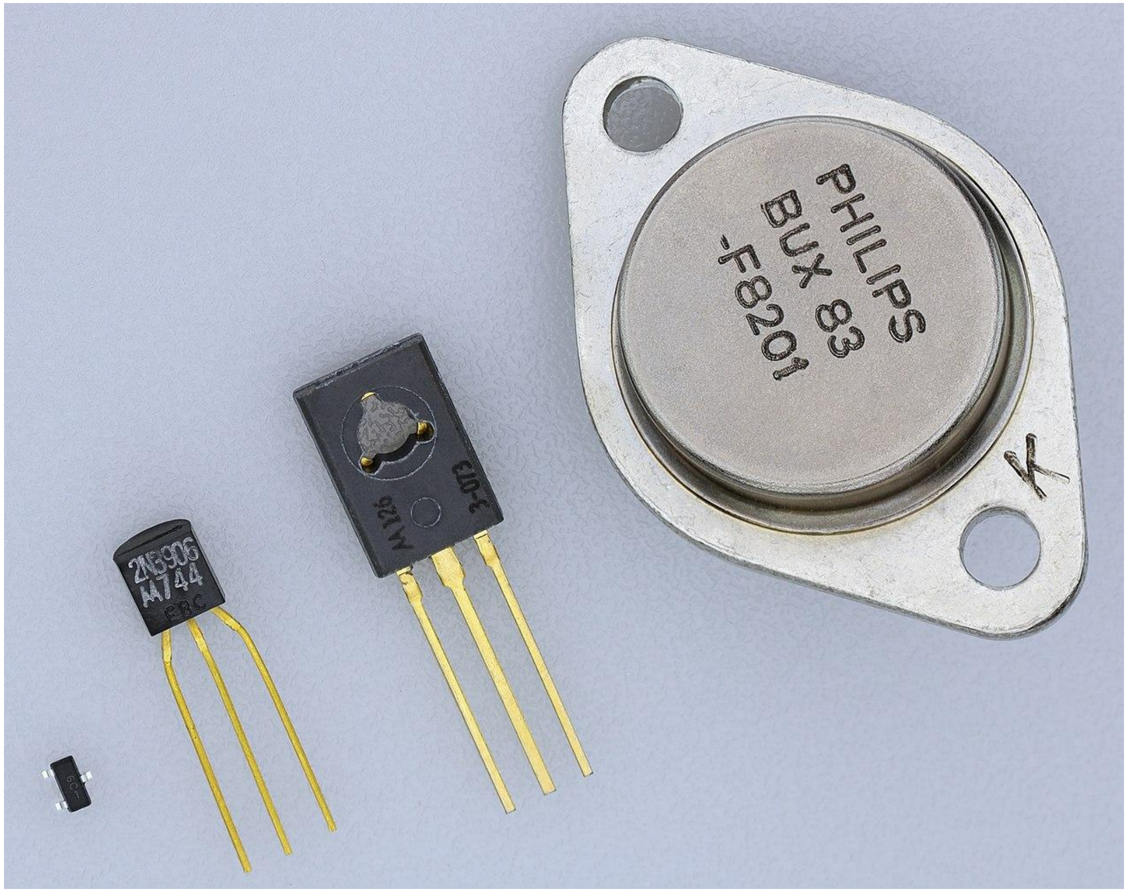
Lecture 3: Analog Electronics
Bipolar Junction Transistors

Dr. Daliso Banda

daliso.banda@unza.zm

Department of Electrical & Electronic Engineering, School of Engineering, University of Zambia

Introduction

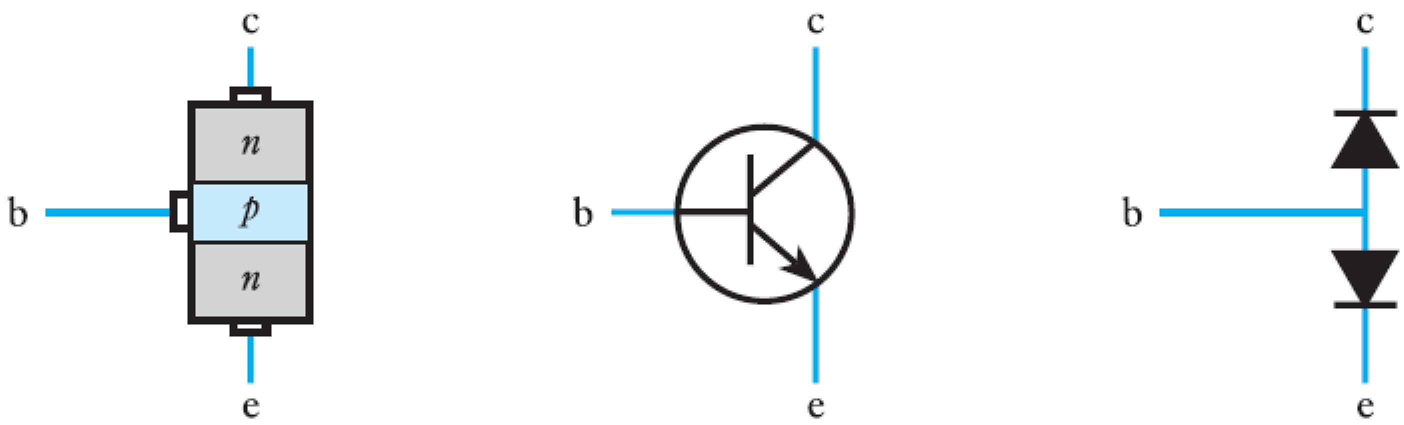


- On December 23, 1947, Dr. S. William Shockley, Dr. Walter H. Brattain and Dr. John Bardeen demonstrated the amplifying action of the first transistor at the Bell Telephone Laboratories.
- Note that this lecture introduces a device with three terminals. You will find that all amplifiers have at least three terminals, with one controlling the flow or potential between the other two.

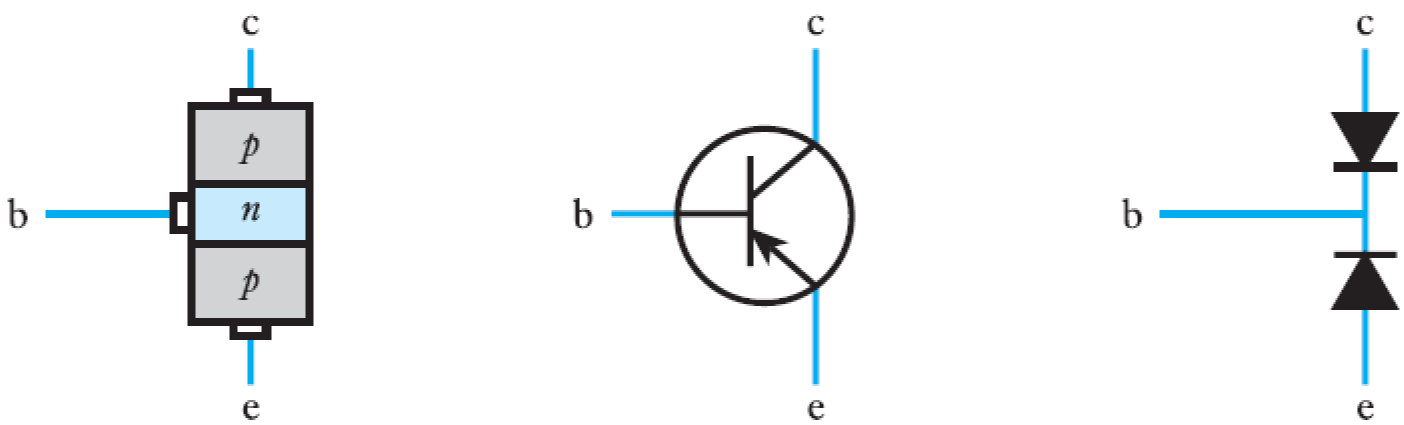
Introduction

- Bipolar Junction Transistors (BJTs) are the main building blocks in electronic systems and are used in both analogue and digital applications.
- BJTs get their name *bipolar* from the fact that the current is carried by both polarities of charges, that is, by both electrons and holes, unlike Field Effect Transistors (FETs) which are *unipolar*.

Introduction



(a) An *npn* transistor



(b) A *pnp* transistor

Transistor Construction

- The transistor is a three-layer semiconductor device consisting of either two *n*- and one *p*-type layers of material or two *p*- and one *n*-type layers of material.
- The former is called an *npn* transistor and the latter is called a *pnp* transistor.
- Fig. 1 shows both transistors with the proper dc biasing.

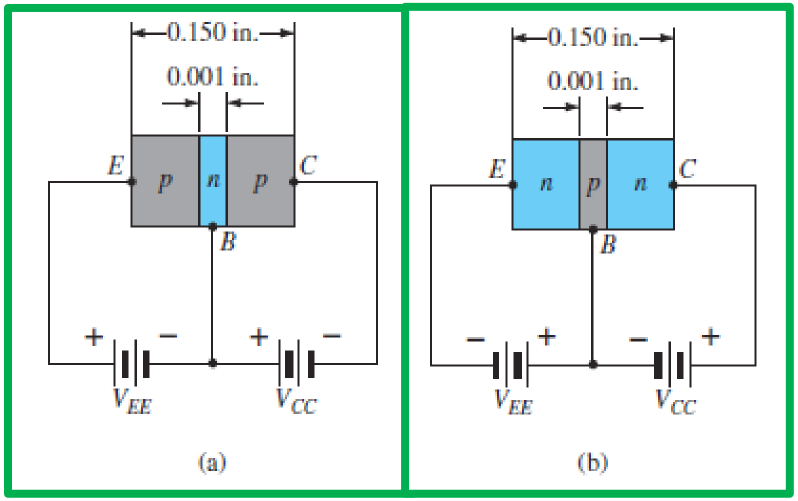
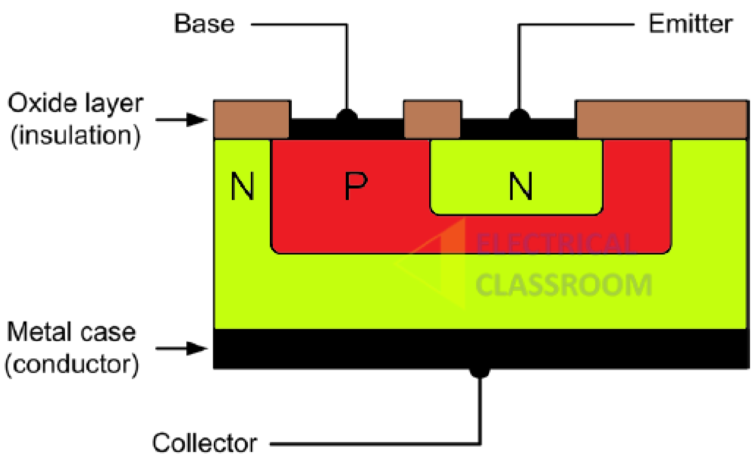


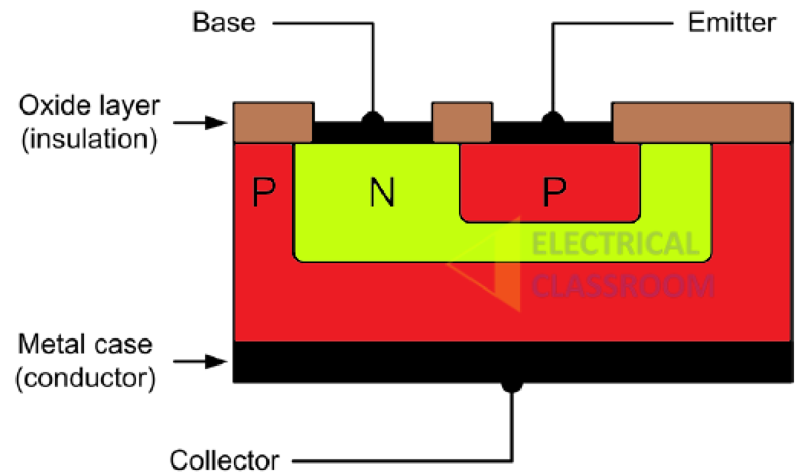
Figure 1: Types of transistors: (a) *pnp*; (b) *npn*.

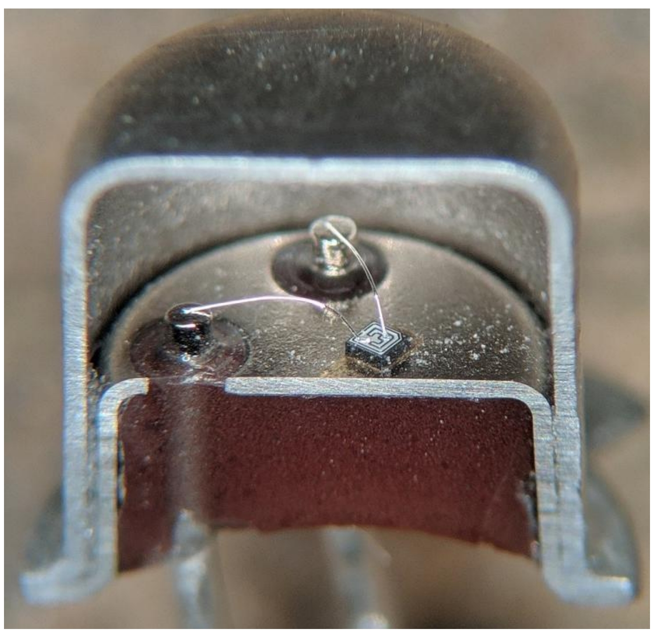
- In lecture 4, we will find that dc biasing is necessary to establish the proper region of operation for ac amplification.
- The Emitter layer, E is heavily doped, with Base, B and Collector, C only lightly doped.
- The lower doping level decreases the conductivity of this material by limiting the number of "free" carriers.

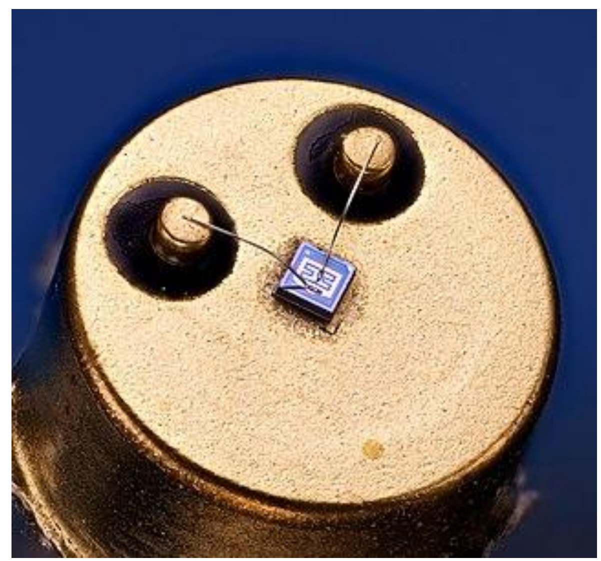
Transistor Construction

- Example transistor structure.



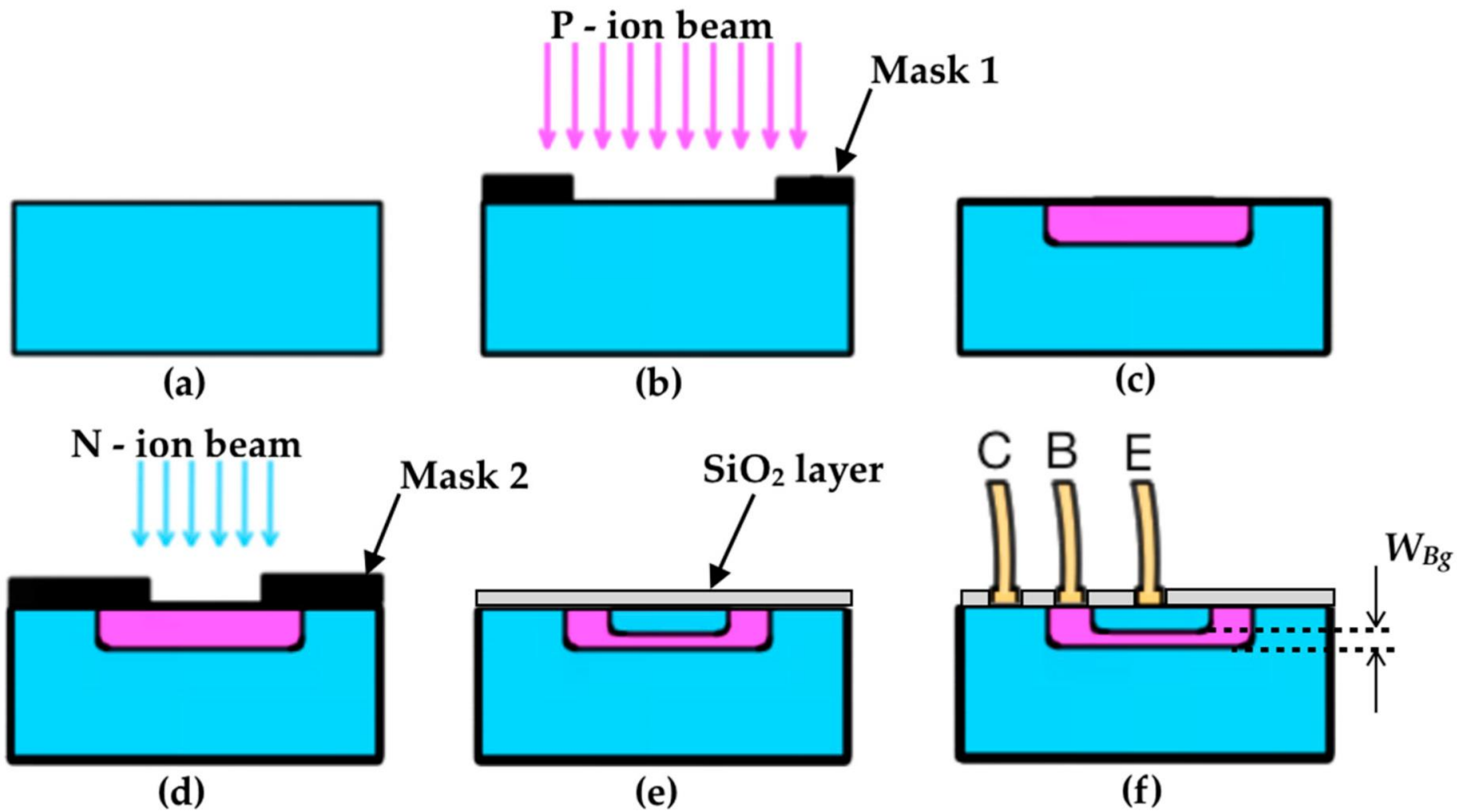






Transistor Construction

- Transistor based ICs are manufactured using Photolithography.
- Photolithography is an optical means of transferring a pattern on a substrate.



Transistor Operation

- We will describe the basic operation of the transistor using the *pnp* transistor of Fig. 1a.
- Notice that the operation of *npn* transistor is exactly the same if the roles of played by the electron and hole are interchanged.
- In Fig. 2a the pnp BJT is redrawn without the base-to-collector bias.
- Note the similarity with the forward-biased diode in lecture 1. The depletion region has been reduced in width resulting in a heavy flow of majority carries from *p*- to the *n*-type material.

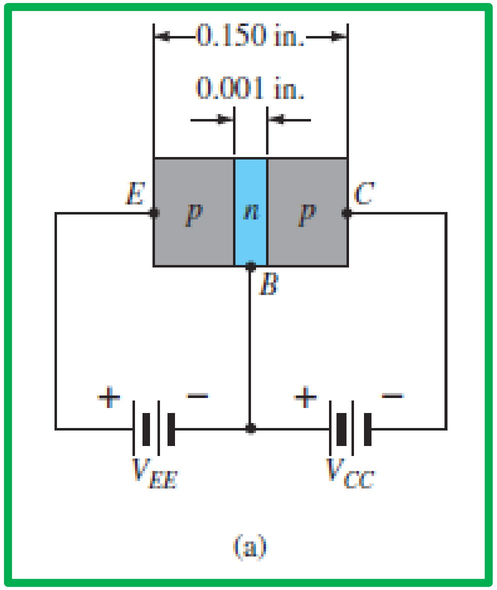


Figure 1: Types of transistors: (a) *pnp*

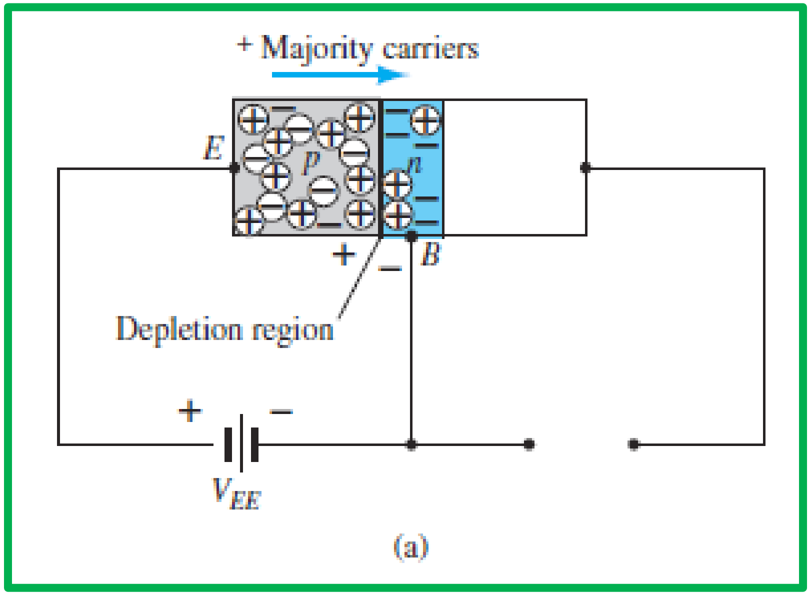


Figure 2: Biasing a transistor: (a) forward-bias

Transistor Operation

- Now remove the base-to-emitter bias of the *pnp* BJT of Fig. 1a as shown in Fig. 2b.
- Notice the similarity with a reverse-biased diode, and recall that the flow of majority carriers is zero and only minority-carrier flow is present.
- Simply put, One p-n junction of a transistor is reversed-biased, whereas the other is forward-biased.

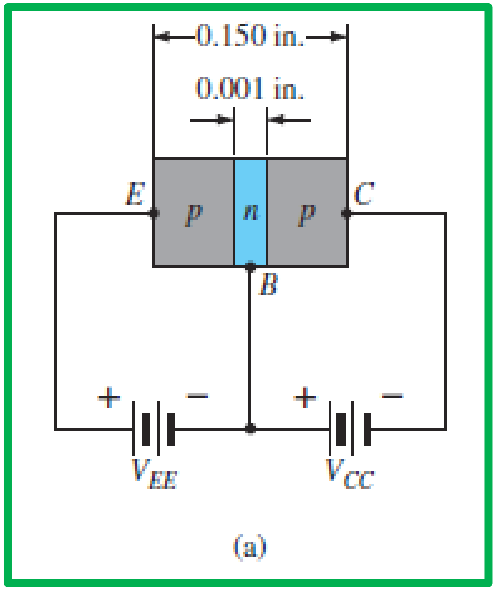


Figure 1: Types of transistors: (a) *pnp*

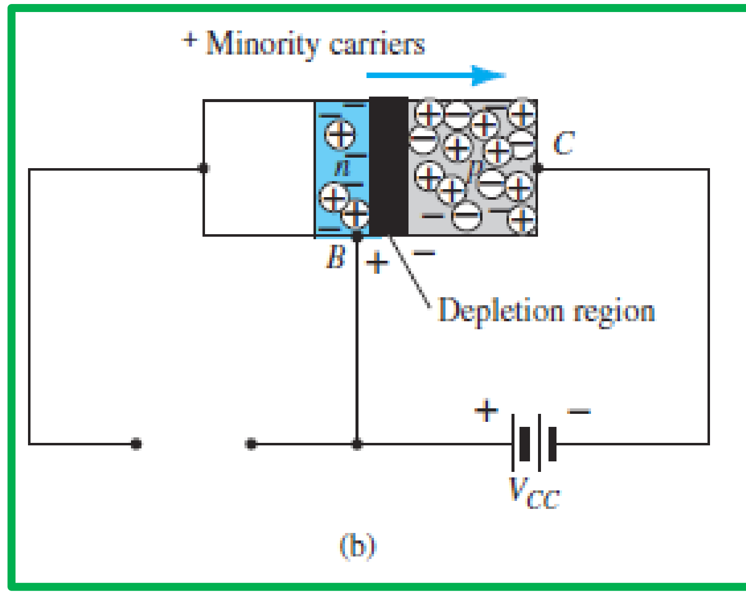


Figure 2: Biasing a transistor (b) reverse-bias.

Transistor Operation Cont'd

- One p-n junction of a transistor is reversed-biased, whereas the other is forward-biased.
- In Fig. 3 both biasing potentials have been applied with the resulting majority- and minority-carrier flow indicated.
- Since the sandwiched *n*-type material (base) is very thin and has low conductivity, a very small number of majority carriers will take this path of high resistance to the base terminal.
- Magnitude of base current is typically on the order of microamperes compared to milliamperes for Emitter and Collector current

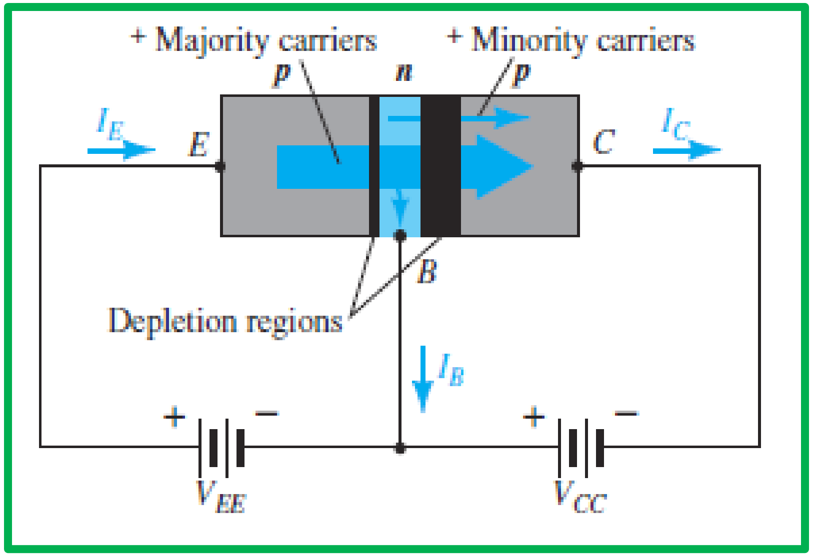


Figure 3: Majority and minority carrier flow of a *pnp* BJT.

Transistor Operation Cont'd

- The bulk of the majority carriers will diffuse across the reverse-biased junction with relative ease because these injected carries will appear as minority carriers in the *n*-type material.
- Combining this with the fact that all minority carriers in the depletion region will cross the reverse-biased junction of a diode accounts for the flow indicated in Fig. 3.
- Applying Kirchhoff's current law (KCL) to the BJT of Fig. 3 as if it were a single node yields

$$I_E = I_C + I_B \quad [1]$$

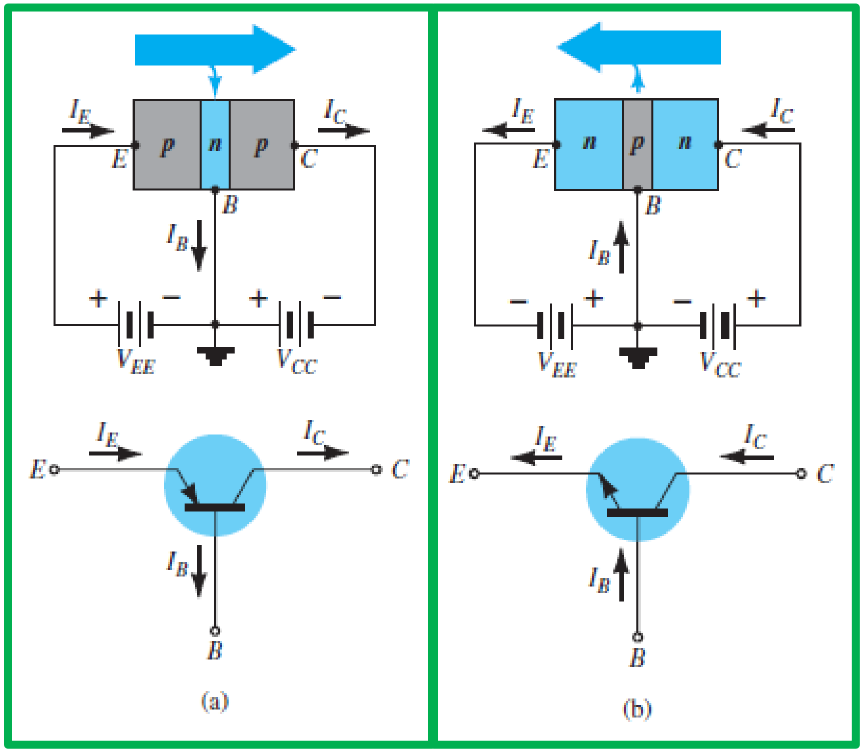
- Notice that the collector current has two components given by

$$I_C = I_{C,\text{majority}} + I_{CO,\text{minority}} \quad [2]$$

- where I_C is measured in milliamperes, and I_{CO} also called *leakage current* is measured in microamperes or nanoamperes.

Common-Base Configuration

- Fig. 4 shows the BJT notation and symbols commonly used in practice for the common-base configuration with *pnp* and *npn* transistors.
- Common base terminology refers to the fact that the base is common to both the input and output. In addition the base is usually the terminal closest to ground potential.



- Throughout our lecture all current directions will refer to conventional (hole) flow rather than electron flow.
- For the BJT the arrow in the graphic symbol defines the direction of emitter current (conventional flow) through the device.

Figure 4: Common-base Configuration: (a) *pnp* transistor; (b) *npn* transistor.

Common-Base Configuration Cont'd

- To describe the behavior of the common-base amplifier of Fig. 4 two sets of characteristics are required.
- One for the driving point or input parameters and the other for the output side.
- The input set as shown in Fig. 5 relates an input current (I_E) to an input voltage (V_{BE}) for various levels of output voltage (V_{CB}).

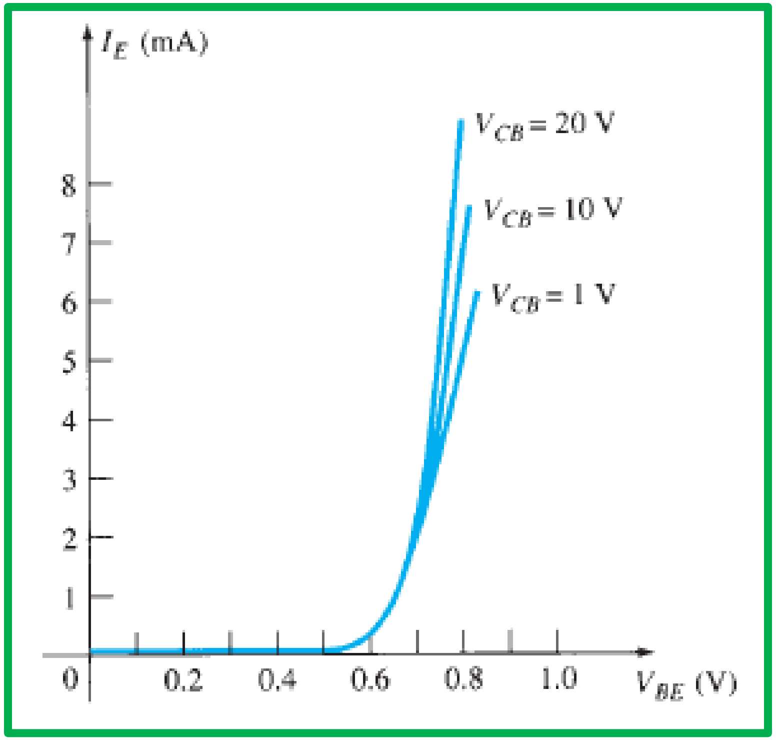


Figure 5: Input or driving point characteristics for a common-base silicon transistor amplifier.

Common-Base Configuration Cont'd

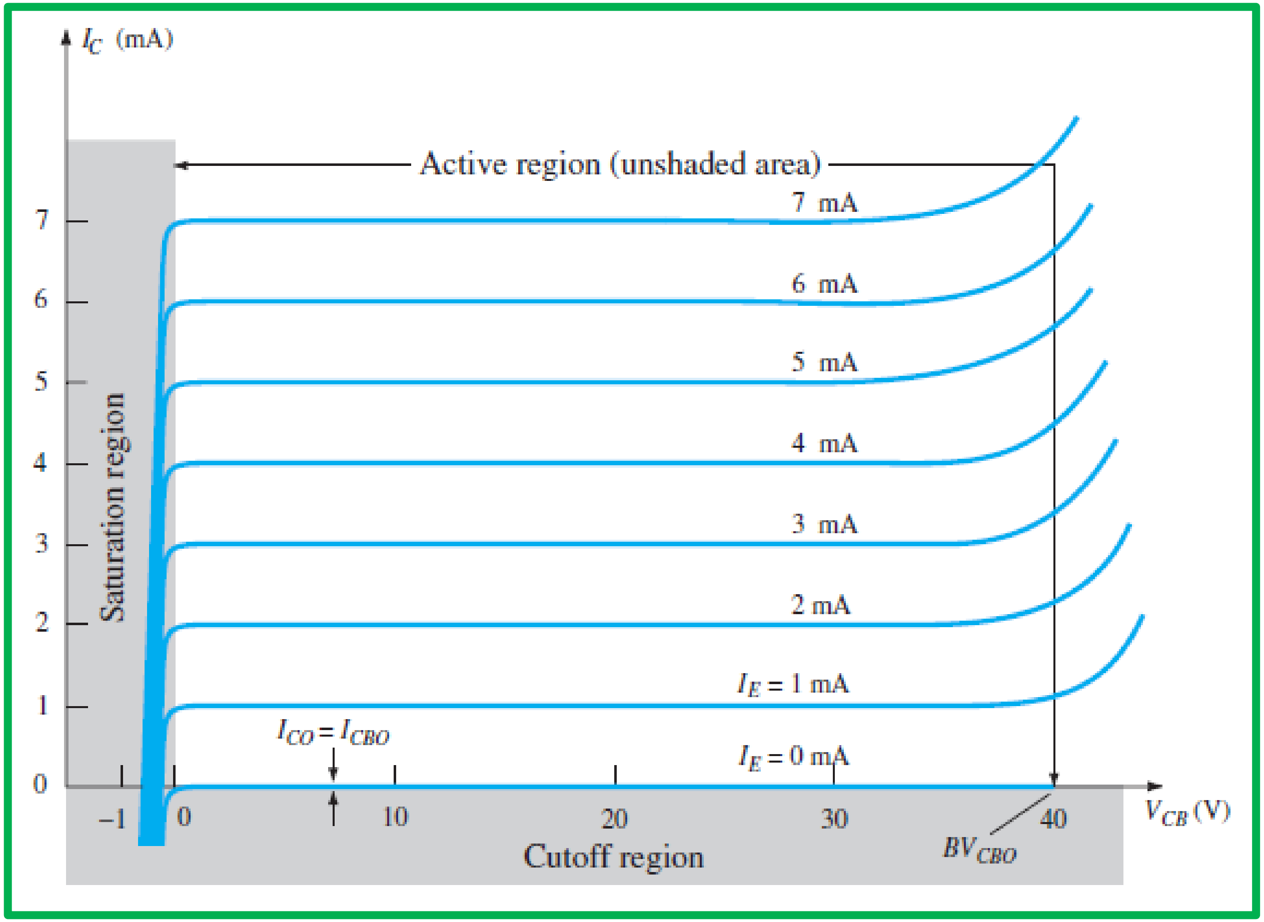


Figure 6: Output or collector characteristics for a common-base transistor amplifier.

- The output set relates an output current (I_C) to an output voltage (V_{CB}) for various input current (I_E) as shown in Fig. 6.
- The output or collector set of characteristics has three basic regions namely: the active, cutoff, and saturation regions.

Common-Base Configuration Cont'd

- In the active region the base-emitter junction is forward biased, whereas the collector base junction is reverse-biased.
- The notation most frequently used for I_{CO} on data and specification sheets is I_{CBO} (the collector-to-base current with the emitter leg open).
- Fig. 3.6 shows that as $I_E \uparrow$ above zero, the $I_C \uparrow$ to a magnitude essentially equal to that of I_E as determined by basic BJT current relations. Thus, we have the approximation in the active region of

$$I_C \cong I_E$$

[3]

- In the cutoff region the base-emitter and collector-base junctions of a transistor are both reverse-biased. Thus, $I_C = 0\ \text{A}$.
- The saturation region is that region of the characteristics to the left of $V_{CB} = 0\ \text{V}$.
- In the saturation region the base-emitter and collector-base junctions are forward-biased.

Common-Base Configuration Cont'd

- Notice that drive-point characteristics of Fig. 5 are affected very little by increase in (V_{CB}) . Thus, like the diode, approximate models can be used

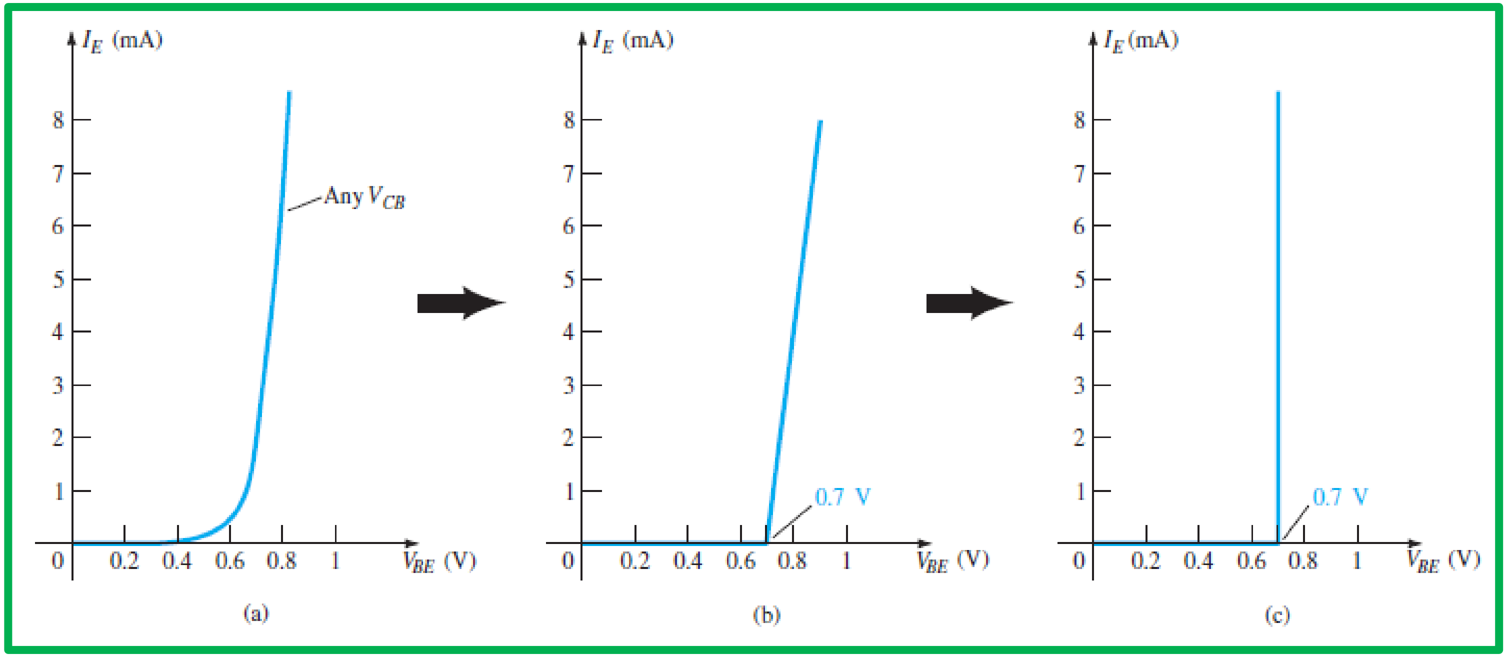


Figure 7: Equivalent model to be employed for the base-to-emitter region of an amplifier in the dc mode.

- Once a transistor is in the "on" state, the base-to-emitter voltage will be assumed to be

$$V_{BE} \cong 0.7\,\text{V}$$

[4]

Example Common-Base Configuration

a) Using the characteristics of Fig. 6, determine the resulting collector current if $I_E = 3\,\text{mA}$ and $V_{CB} = 10\,\text{V}$.

b) Using the characteristics of Fig. 6, determine the resulting collector current if I_E remains at $3\,\text{mA}$ but V_{CB} is reduced to $2\,\text{V}$.

c) Using the characteristics of Fig. 5 and 6, determine V_{BE} if $I_C = 4\,\text{mA}$ and $V_{CB} = 20\,\text{V}$

b) Repeat part (c) using the characteristics of Fig. 6 and 7c.

[Solution]

a) The characteristics clearly indicate that $I_C \cong I_E = \mathbf{3\,mA}$.

b) The effect of changing V_{CB} is negligible and I_C continues to be $\mathbf{3\,mA}$.

c) From Fig. 3.6, $I_E \cong I_C = 4\,\text{mA}$. On Fig. 5 the resulting level of V_{BE} is about $\mathbf{0.74\,V}$.

d) Again from Fig. 3.6, $I_E \cong I_C = 4\,\text{mA}$. However, on Fig. 7c, V_{BE} is $\mathbf{0.7\,V}$ for any level of emitter current.

Common-Base Configuration Cont'd

Alpha (α)

- **DC Mode** In dc mode the levels of I_C and I_E due to the majority carriers are related by a quantity called *alpha* and defined by the following equation:

$$\alpha_{dc} = \frac{I_C}{I_E} \quad [5]$$

- where I_C and I_E are levels of current at the point of operation.
- Much as Fig. 6 suggests that $\alpha = 1$, practical devices have $0.90 \le \alpha \le 0.998$.
- Since alpha is defined solely for majority carriers, Eq. (2) becomes

$$I_C = \alpha I_E + I_{CBO} \quad [6]$$

- **AC Mode** For ac situations where the point of operation moves on the characteristic curve, an ac alpha (common-base, short-circuit, amplification factor) is defined by

$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}} \quad [7]$$

Common-Base Configuration Cont'd

Biasing

- Proper biasing of common-base configuration in the active region can be determined quickly using $I_C \cong I_E$ and assuming for the moment that $I_B = 0\ \mu A$. This results in Fig. 8.

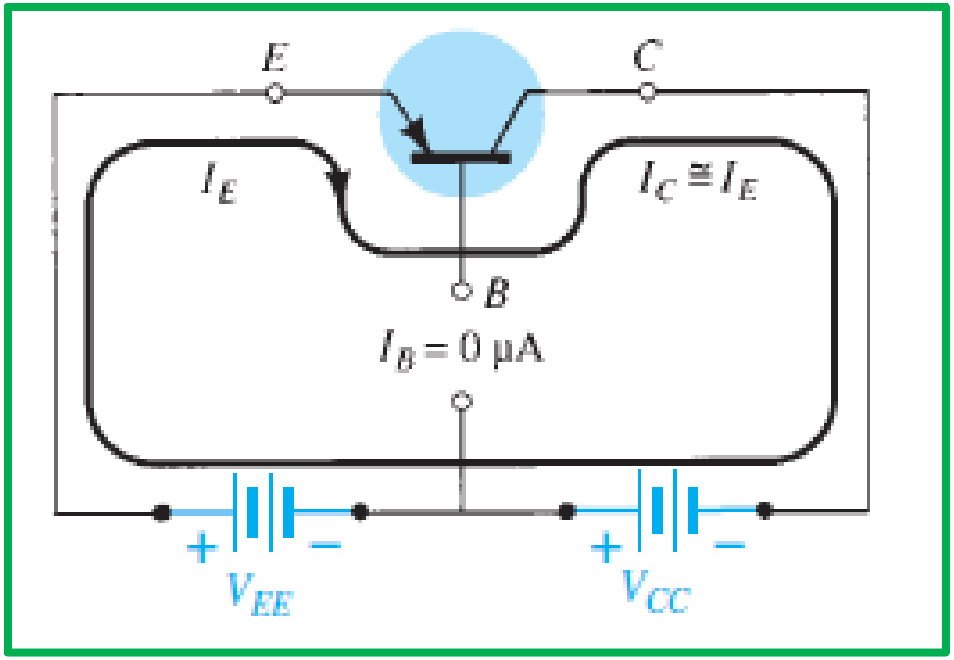
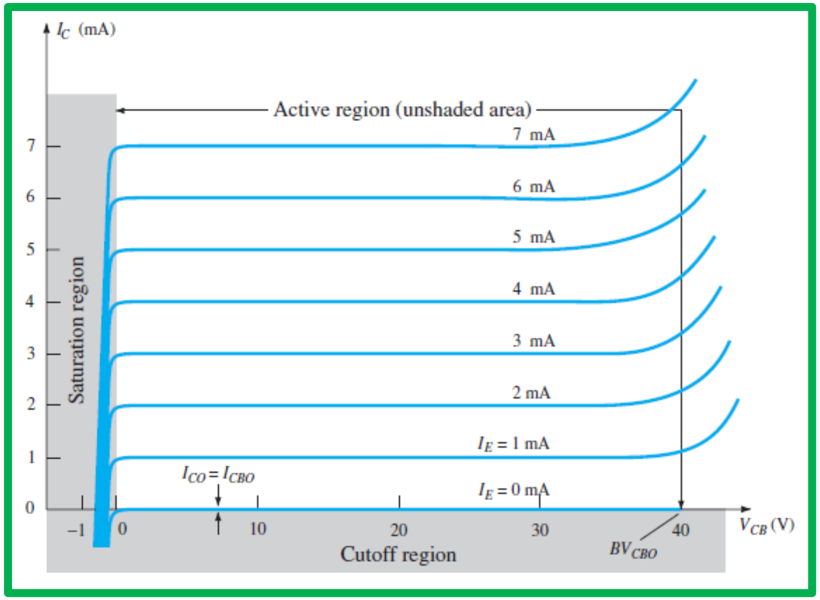
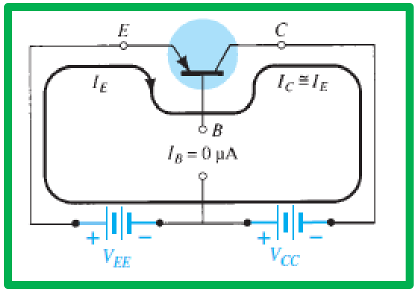


Figure 8: Establishing the proper biasing management for a common-base *pnp* transistor in the active region.

Common-Base Configuration Cont'd





Breakdown Region

- As applied voltage V_{CB} increases there is a point where the curves take a dramatic upswing in Fig. 6.
- This is primarily due to an avalanche effect similar to that described for the diode in lecture 1.
- The largest permissible base-to-collector voltage is labeled BV_{CBO} as shown in Fig. 6. It is also referred to as $V_{(BR)CBO}$.
- Note that this limitation is only for the common-base configuration.

Common-Emitter Configuration

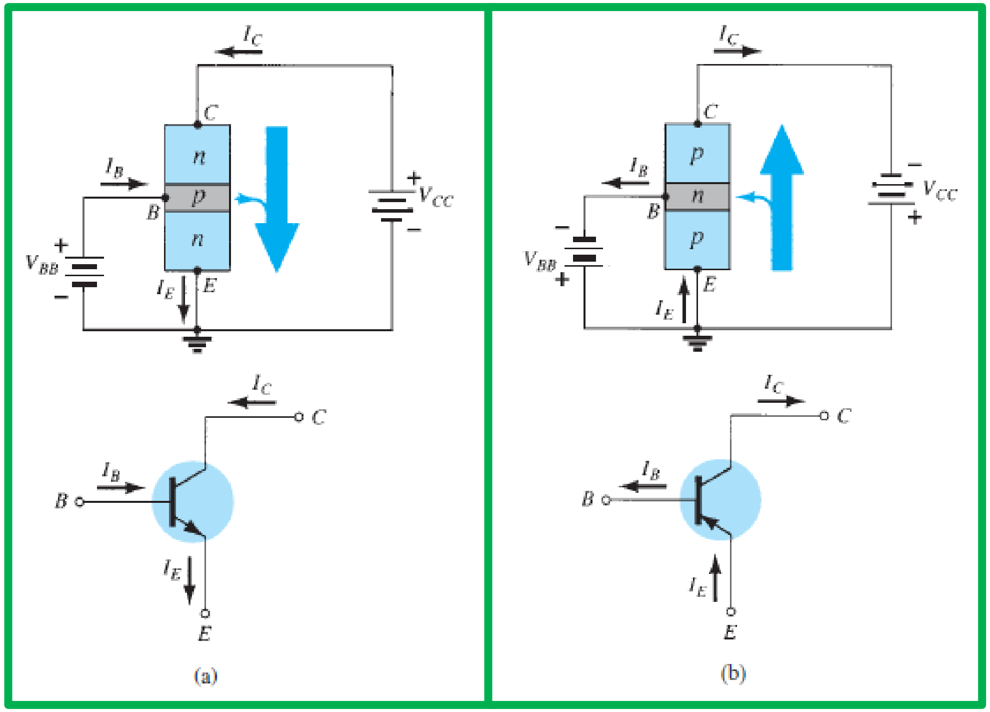


Figure 9:
Common-emitter configuration:
(a) *npn* transistor; (b) *pnp* transistor.

- Common-emitter configuration because the emitter is common to both the input (base) and output (collector) terminals.
- Two sets of characteristics are once again necessary to describe fully its behavior: one for the input or base-emitter circuit and one for the output or collector-emitter circuit.

Common-Emitter Configuration Cont'd

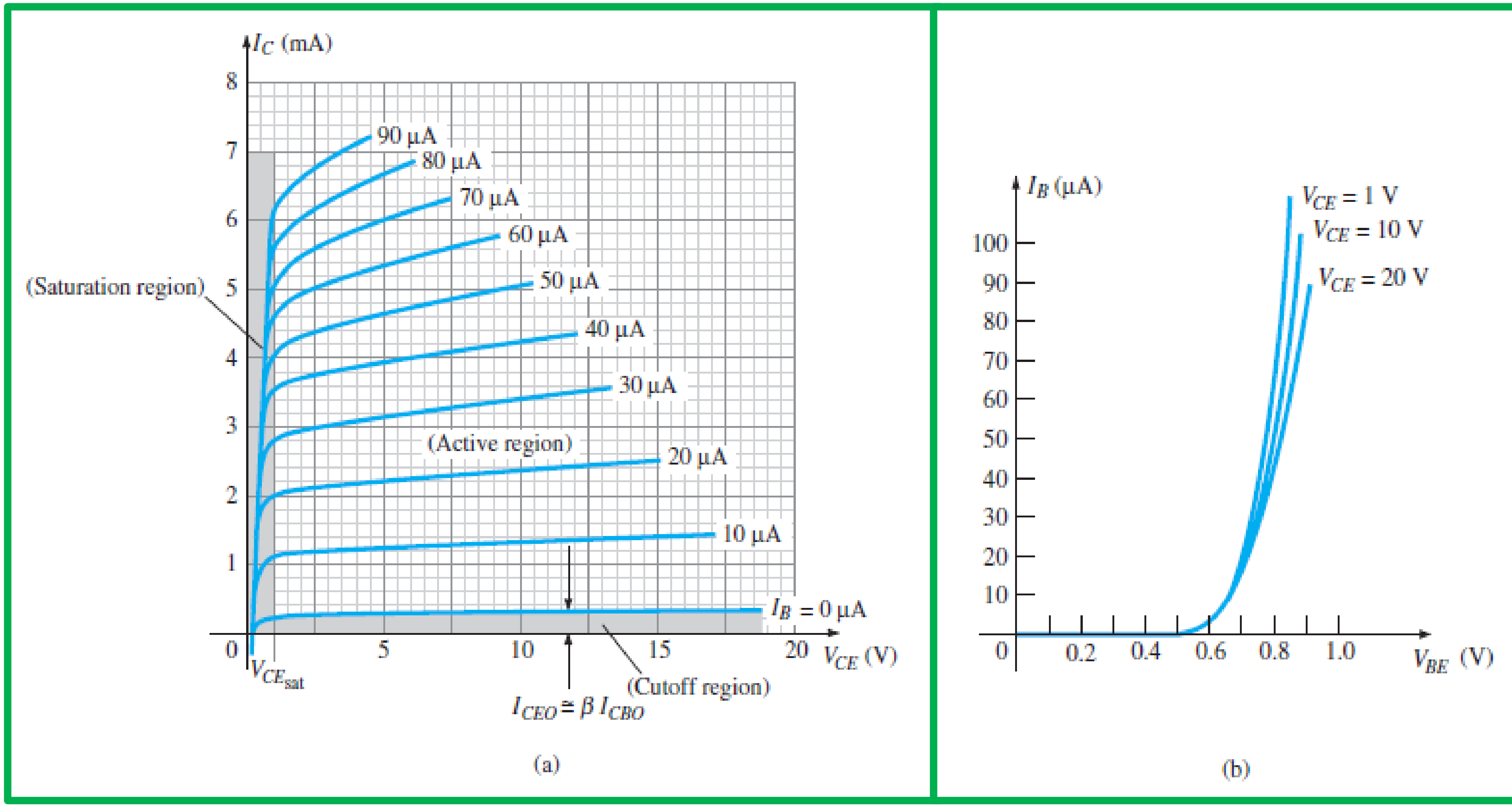
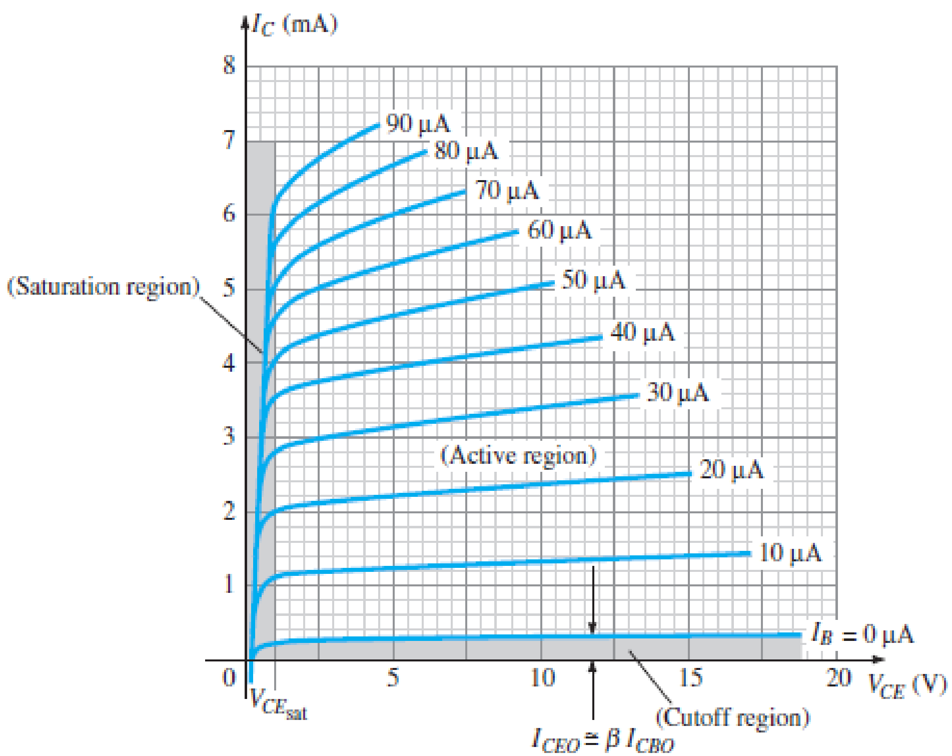
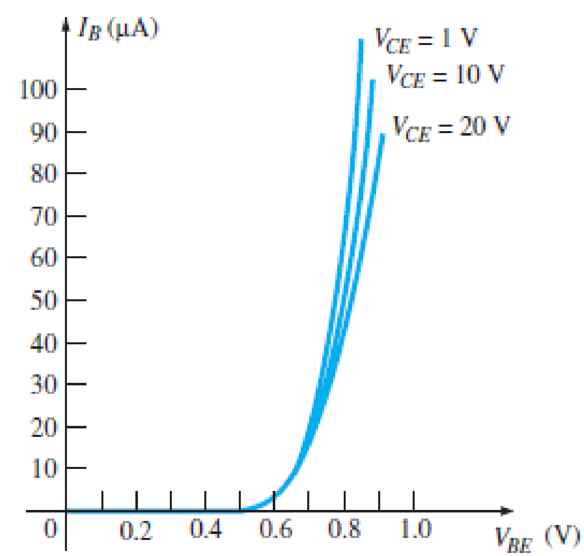


Figure 10: Characteristics of a silicon BJT in the common-emitter configuration: (a) collector characteristics; (b) base characteristics.

Common-Emitter Configuration Cont'd

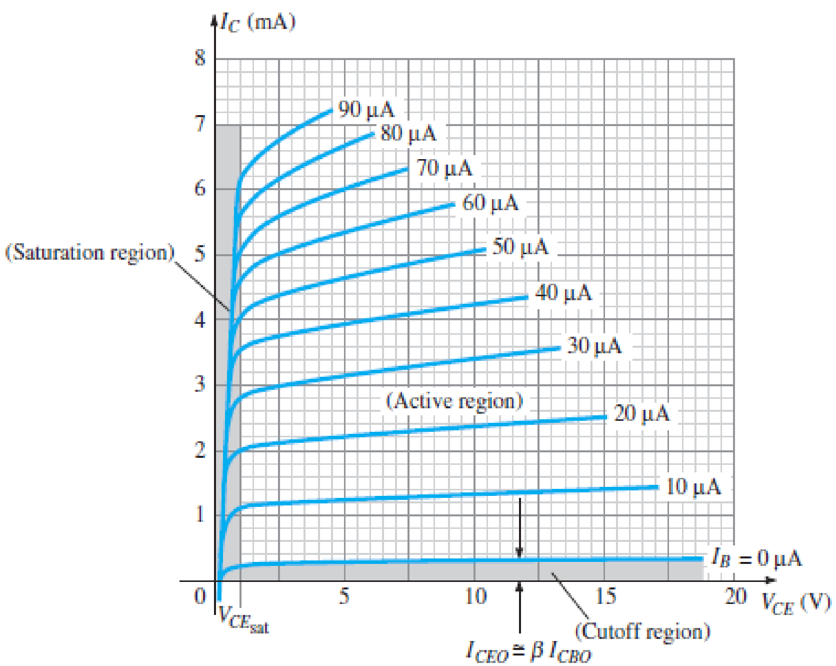
- Notice that applying Kirchhoff's current law to Fig. 9 yields, $I_E = I_C + I_B$ and $I_C = \alpha I_E$, like was found in the common-base configuration.
- Here the output characteristics are a plot of output current (I_C) versus output voltage (V_{CE}) for a range of values of input current (I_B).
- The input characteristics are a plot of input current (I_B) versus the input voltage (V_{BE}) for a range of values of the output voltage (V_{CE}).

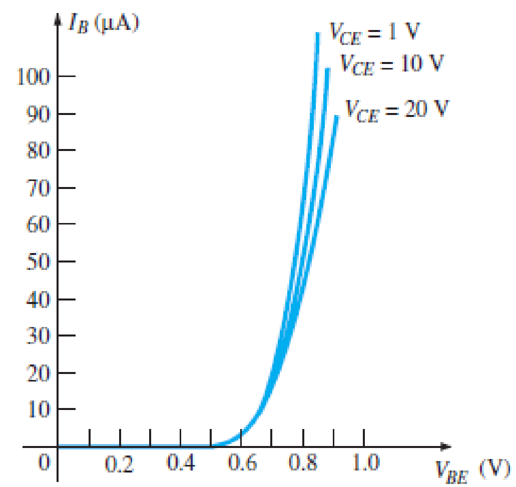




Common-Emitter Configuration Cont'd

- Note that the magnitude of I_B is in microamperes, compared to milliamperes of I_C .
- Furthermore, the curves of I_B in Fig. 10a are not horizontal which entails that V_{CE} will influence the magnitude of collector current.
- In the active region of a common-emitter amplifier, the base-emitter junction is forward-biased, whereas the collector-base junction is reverse-biased.
- The active region of the common-emitter configuration can be employed for voltage, current, or power amplification.





Common-Emitter Configuration Cont'd

- The cutoff region for the common-emitter configuration is not as well defined as for the common-base configuration.
- Note on the collector characteristic of Fig. 3.10 that $I_C \neq 0\ \text{A}$ when $I_B = 0\ \text{A}$.
- The collector characteristics can thus be derived through manipulation of Eqs. [1] and [6]. That is,

Eq. [3.6]: $I_C = \alpha I_E + I_{CBO}$

Substitution gives Eq. [3.1]: $I_C = \alpha\left(I_C + I_B\right) + I_{CBO}$;

Rearranging yields

$$I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO} \qquad \textbf{[8]}$$

- Now we let $I_B = 0\ \text{A}$, and substitute a typical value $\alpha = 0.996$, this yields,

$$I_C = \left(\frac{\alpha}{1-\alpha}\right)(0\ \text{A}) + \left(\frac{1}{1-0.996}\right) I_{CBO}\ ; \quad \Rightarrow \quad I_C = \frac{I_{CBO}}{0.004} = 250 I_{CBO}$$

- If we let $I_{CBO} = 1\ \mu\text{A}$, the resulting collector current with $I_B = 0\ \text{A}$ would be $I_{CBO} = 250\left(1\ \mu\text{A}\right) = 0.25\ \text{mA}$, as shown in Fig. 10.

Common-Emitter Configuration Cont'd

- Thus for future reference, note that the collector current for $I_B = 0\ \mu A$ is given by

$$I_{CEO} = \left.\frac{I_{CBO}}{1-\alpha}\right|_{I_B = 0\ \mu A}$$

[9]

- For linear (least distortion) amplification purposes, cutoff for the common-emitter configuration will be defined by $I_C = I_{CEO}$.
- When employed as a switch in the logic circuitry of a computer, a transistor will have two points of operation of interest: one in the cutoff and one in the saturation region.
- For the common-emitter configuration the input set of characteristics can be approximated by a straight-line equivalent depicted in Fig. 3.11.

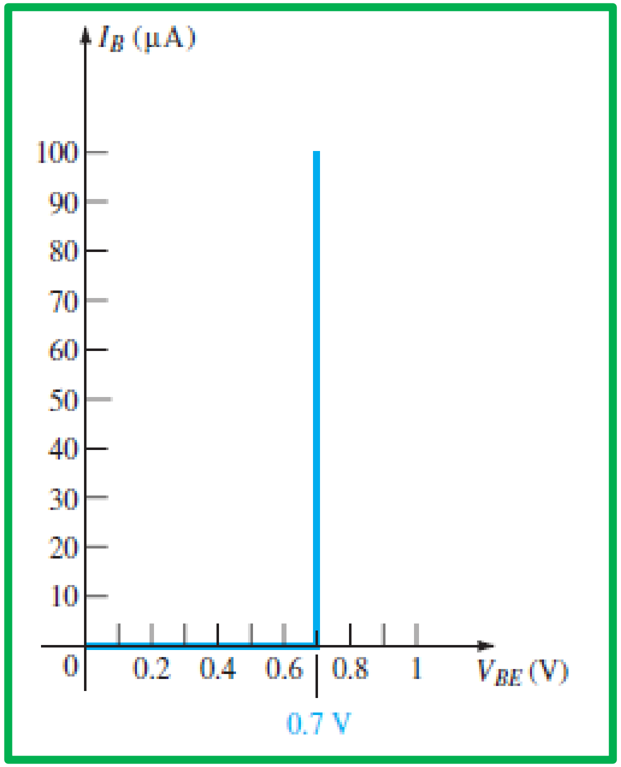


Figure 11 Piecewise-linear equivalent for the diode characteristics.

Example Common-Emitter Configuration

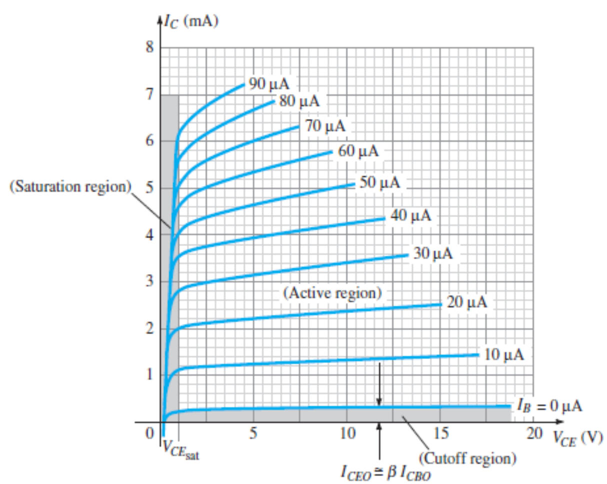
a) Using the characteristics of Fig. 10, determine I_C at $I_B = 30\ \mu A$ and $V_{CE} = 10\ V$.

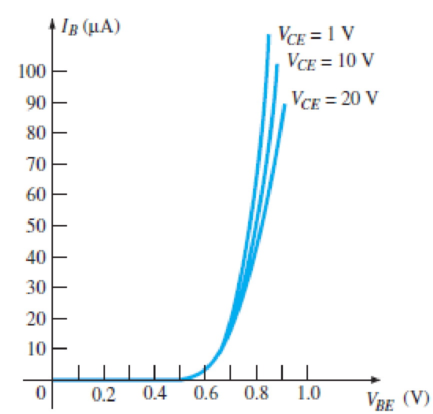
b) Using the characteristics of Fig. 10, determine I_C at $V_{BE} = 0.7\ V$ and $V_{CE} = 15\ V$

[Solution]

a) At the intersection of $I_B = 30\ \mu A$ and $V_{CE} = 10\ V$, $I_C = \mathbf{3.4\ mA}$

b) Using Fig. 3.10b, we obtained $I_B = 20\ \mu A$ at the intersection of $V_{BE} = 0.7\ V$ and $V_{CE} = 15\ V$. From Fig. 3.10a we find that $I_C = \mathbf{2.5\ mA}$ at the intersection of $I_B = 20\ \mu A$ and $V_{CE} = 15\ V$.





Common-Emitter Configuration Cont'd

Beta (β)

- **DC Mode** In the dc mode the levels of I_C and I_B are related by a quantity called beta and defined by

$$\beta_{\mathrm{dc}} = \frac{I_C}{I_B} \qquad [10]$$

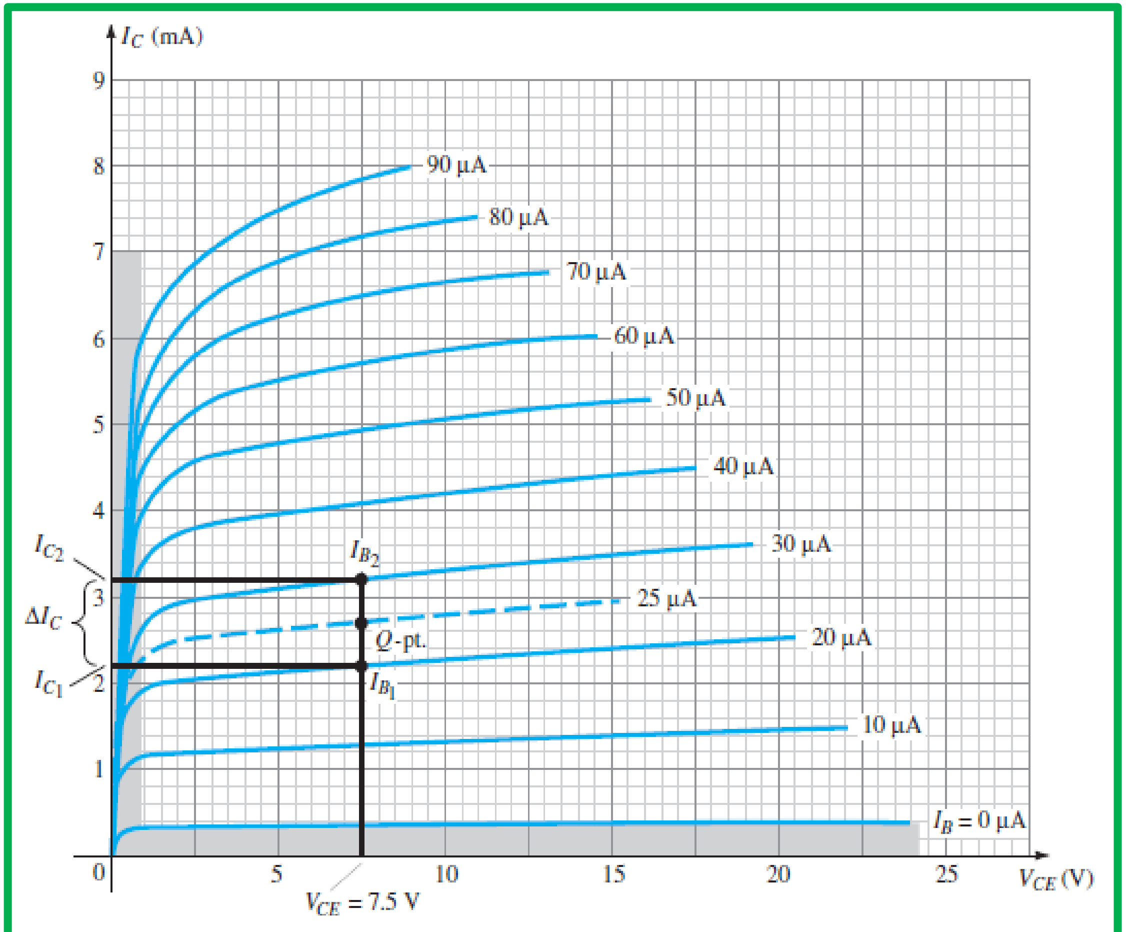
- Where I_C and I_B are determined at a particular operating point on the characteristics.
- Typical values fall in the range $50 \le \beta \le 400$.
- On the specification sheets β_{dc} is usually included as h_{FE} with *h* derived from an ac hybrid equivalent circuit to be discussed latter.
- **AC Mode** For ac situations an ac beta is defined as follows:

$$\beta_{\mathrm{ac}} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\mathrm{constant}} \qquad [11]$$

- $\beta_{\mathrm{ac}} = h_{fe}$ is common-emitter, forward-current, amplification factor.

Common-Emitter Configuration Cont’d

- Let us determine β_{ac} for a region of the characteristics defined by a Q-point of $I_B = 25\ \mu\text{A}$ and $V_{CE} = 7.5\ \text{V}$, as indicated in Fig. 3.12. Clearly



$$\beta_{\text{ac}} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}}$$

$$= \frac{I_{C_2} - I_{C_1}}{I_{B_2} - I_{B_1}} = \frac{(3.2 - 2.2)\,\text{mA}}{(30 - 20)\,\mu\text{A}};$$

$$\beta_{\text{ac}} = \mathbf{100}$$

- At the Q-point,

$$\beta_{\text{dc}} = \frac{I_C}{I_B} = \frac{2.7\,\text{mA}}{25\,\mu\text{A}} = \mathbf{108}$$

Figure 12 Determining β_{ac} and β_{dc} from collector characteristics.

Common-Emitter Configuration Cont'd

- A relationship between β and α is developed as follows. Recall that,

$$\beta = I_C / I_B \; ; \quad \Rightarrow \quad I_B = I_C / \beta \qquad \text{and} \qquad \alpha = I_C / I_E \; ; \quad \Rightarrow \quad I_E = I_C / \alpha$$

- Substituting into

$$I_E = I_C + I_B$$

yields

$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta} \; ; \qquad \Rightarrow \qquad \frac{1}{\alpha} = 1 + \frac{1}{\beta} \; ;$$

thus,

$$\alpha = \frac{\beta}{\beta + 1} \qquad [12]$$

$$\beta = \frac{\alpha}{1 - \alpha} \qquad [13]$$

- Furthermore, recall that $I_{CEO} = \dfrac{I_{CBO}}{1-\alpha} \; ; \; \Rightarrow \; I_{CEO} = (\beta + 1) I_{CBO} \; ;$

$$I_{CEO} \cong \beta I_{CBO} \qquad [14]$$

Common-Emitter Configuration Cont'd

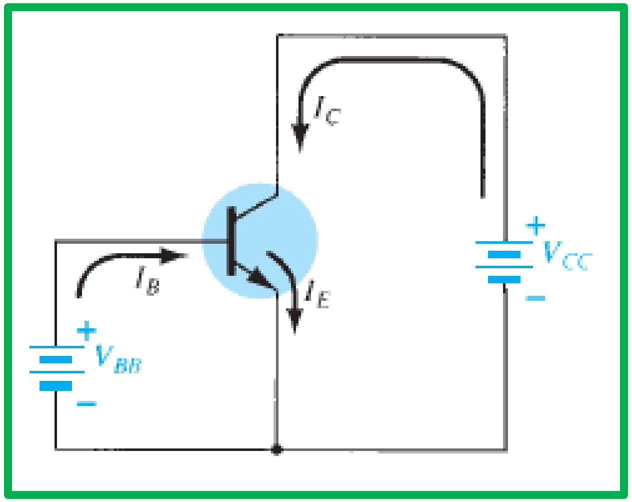
- Notice that beta is an important parameter in that it relates input and output currents for a common-emitter configuration. That is,

$$I_C = \beta I_B \qquad [15]$$

and since $I_E = I_C + I_B \;;\quad \Rightarrow \quad I_E = \beta I_B + I_B$

thus,

$$I_E = (\beta + 1) I_B \qquad [16]$$



Biasing

- Proper biasing of a common-emitter amplifier for an *npn* transistor is such that currents flow as shown in Fig. 3.13.

Figure 13 Proper biasing for common-emitter *npn* transistor configuration.

Common-Emitter Configuration Cont'd

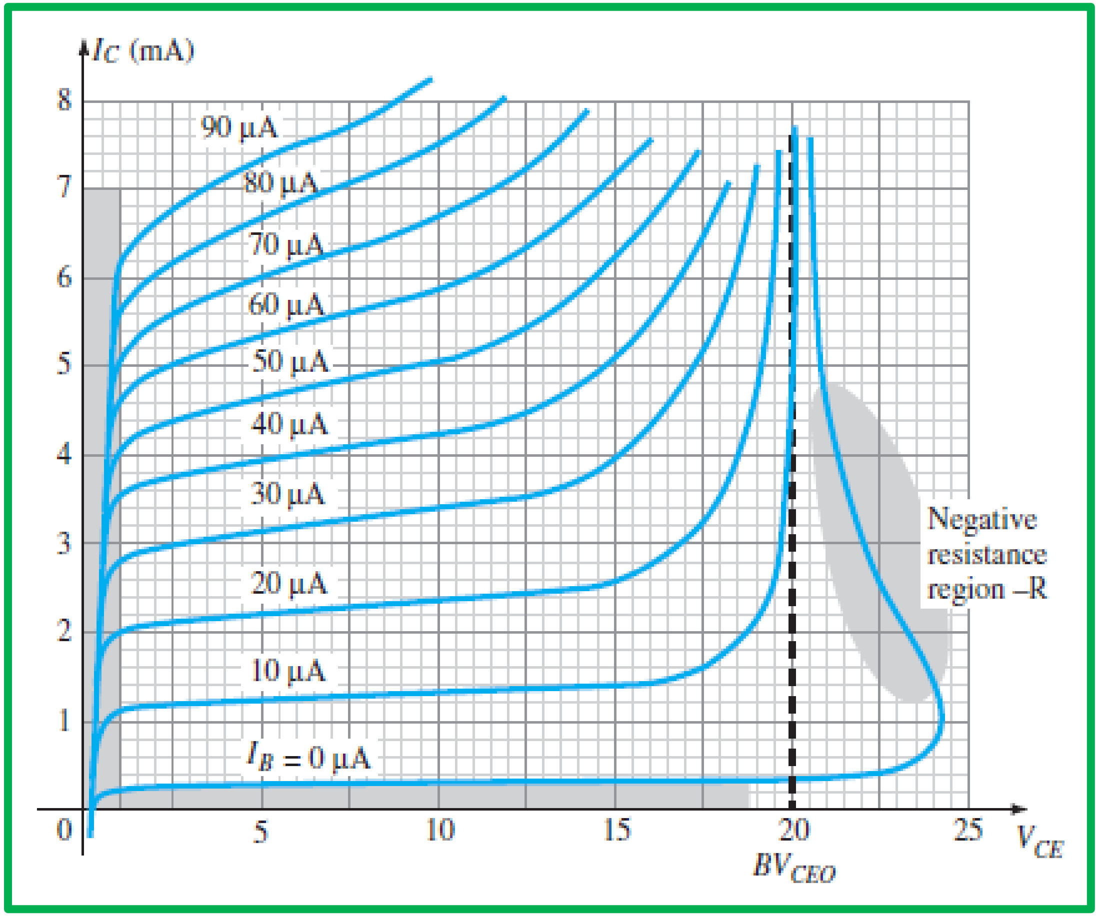


Figure 14 Examining breakdown region of BJT in common-emitter configuration.

Breakdown Region

- There is a maximum V_{CE} that can be applied and still remain in the active stable region of operation
- Noteworthy is the region of negative resistance where an increase in current is resulting in a drop in voltage against all odds for resistive elements.
- The breakdown voltage is labeled BV_{CEO} or $V_{(BR)CEO}$ beyond which avalanche breakdown and punch-through occur.

Common-Collector Configuration

- Use primarily for impedance-matching purposes since it has high input impedance and low output impedance.

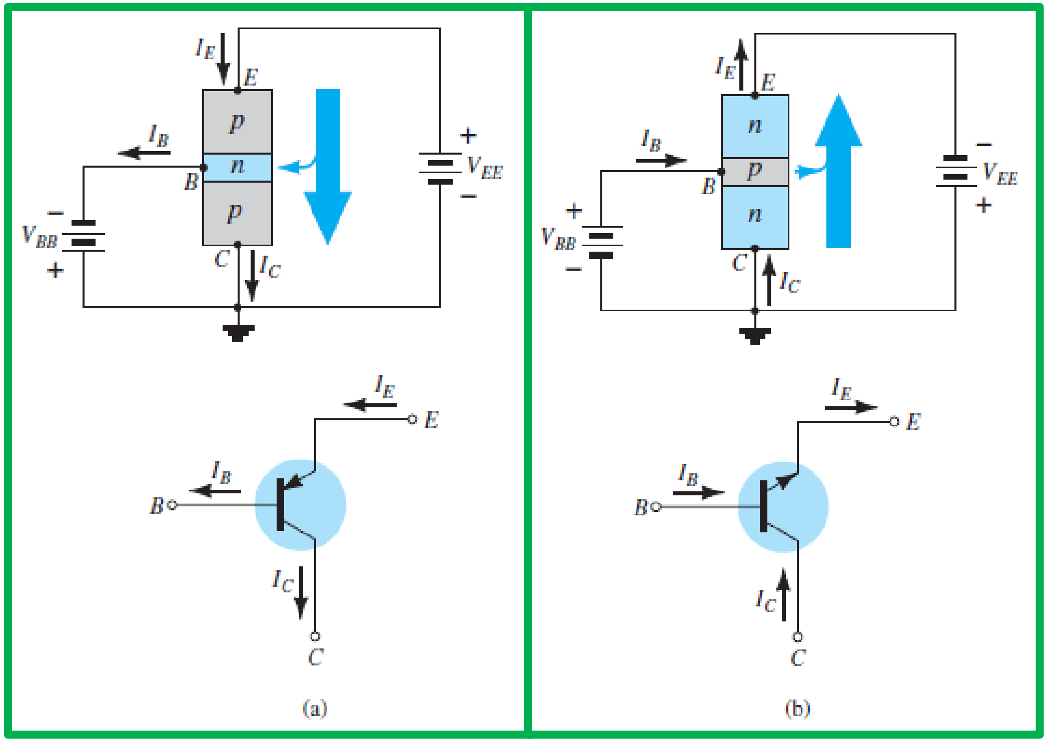
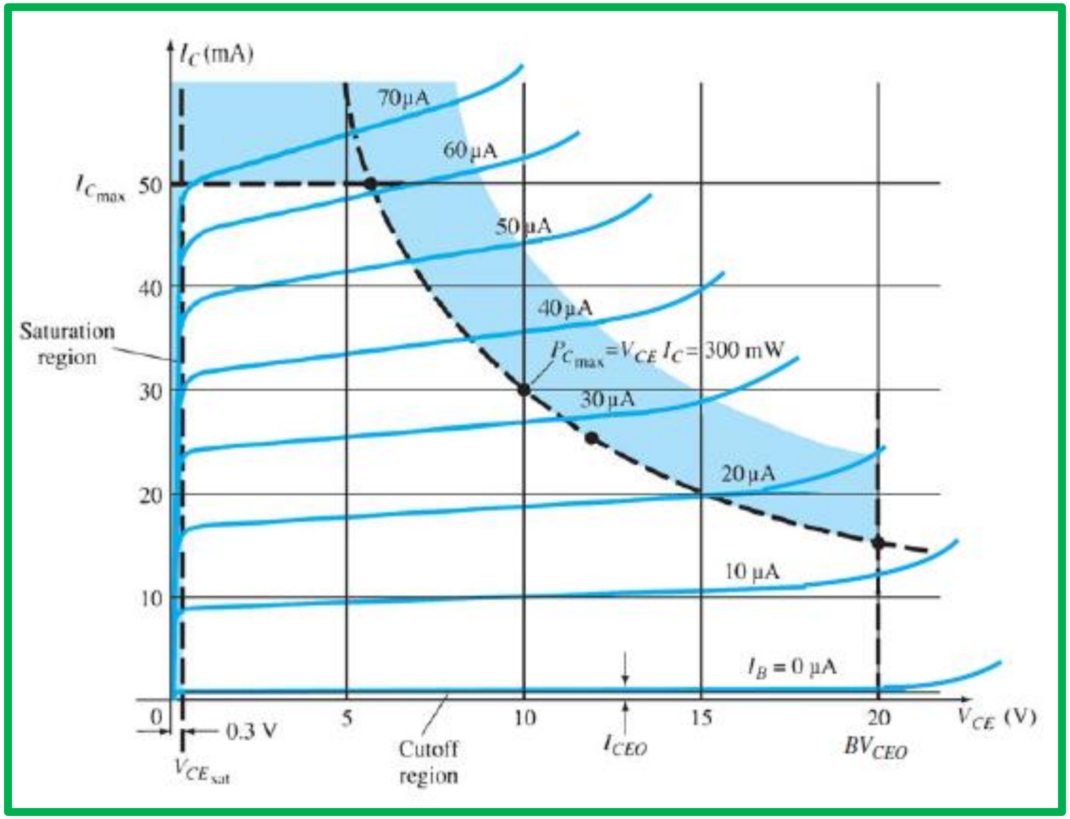


Figure 15 Common-collector configuration: (a) pnp transistor; (b) npn transistor.

- From a design perspective, there is no need for a set of common-collector characteristics as the output characteristics are the same as for the common-emitter configuration.
- Here the horizontal voltage axis is obtained by simply changing the sign of V_{CE} of the common-emitter characteristics.
- I_C and I_E can be interchanged on the vertical axis without any difference.

Limits of Operation

- Some of the limits of operation are self-explanatory, such as maximum collector current (*continuous* collector current) and maximum collector-to-emitter voltage (BV_{CEO} or $V_{(BR)CEO}$).
- The maximum dissipation level is defined by the following equation:



$$P_{C,\max} = V_{CE} I_C \qquad [17]$$

- If characteristics curves are unavailable, simply ensure

$$I_{CEO} \le I_C \le I_{C,\max}$$
$$V_{CE,\text{sat}} \le V_{CE} \le V_{CE,\max} \qquad [18]$$
$$V_{CE} I_C \le P_{C,\max}$$

$$P_{C,\max} = V_{CB} I_C \qquad [19]$$

Figure 16 Defining the linear (undistorted) region of operation for a transistor.

Transistor Specification Sheet

MAXIMUM RATINGS

Rating	Symbol	2N4123	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	625 5.0	mW mW°C
Operating and Storage Junction Temperature Range	T_j, T_{stg}	–55 to +150	°C

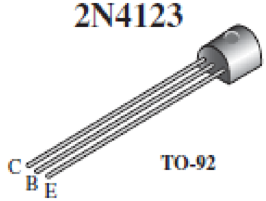
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C W

FAIRCHILD

SEMICONDUCTOR ™

2N4123



General Purpose Transistor NPN Silicon

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) ($I_C = 1.0$ mAdc, $I_E = 0$)	$V_{(BR)CEO}$	30		Vdc
Collector-Base Breakdown Voltage ($I_C = 10$ µAdc, $I_E = 0$)	$V_{(BR)CBO}$	40		Vdc
Emitter-Base Breakdown Voltage ($I_E = 10$ µAdc, $I_C = 0$)	$V_{(BR)EBO}$	5.0	–	Vdc
Collector Cutoff Current ($V_{CB} = 20$ Vdc, $I_E = 0$)	I_{CBO}	–	50	nAdc
Emitter Cutoff Current ($V_{BE} = 3.0$ Vdc, $I_C = 0$)	I_{EBO}	–	50	nAdc
ON CHARACTERISTICS				
DC Current Gain(1) ($I_C = 2.0$ mAdc, $V_{CE} = 1.0$ Vdc) ($I_C = 50$ mAdc, $V_{CE} = 1.0$ Vdc)	h_{FE}	 50 25	 150 –	–
Collector-Emitter Saturation Voltage(1) ($I_C = 50$ mAdc, $I_B = 5.0$ mAdc)	$V_{CE(sat)}$	–	0.3	Vdc
Base-Emitter Saturation Voltage(1) ($I_C = 50$ mAdc, $I_B = 5.0$ mAdc)	$V_{BE(sat)}$	–	0.95	Vdc

Figure 17 Transistor specification sheet.

- It is the communication link between the manufacturer and user.
- Page 146 of [2] shows an example of specification sheet provided by Fairchild Semiconductor Corporation for 2N4123 *npn* transistor.

Transistor Casing and Terminal Identification

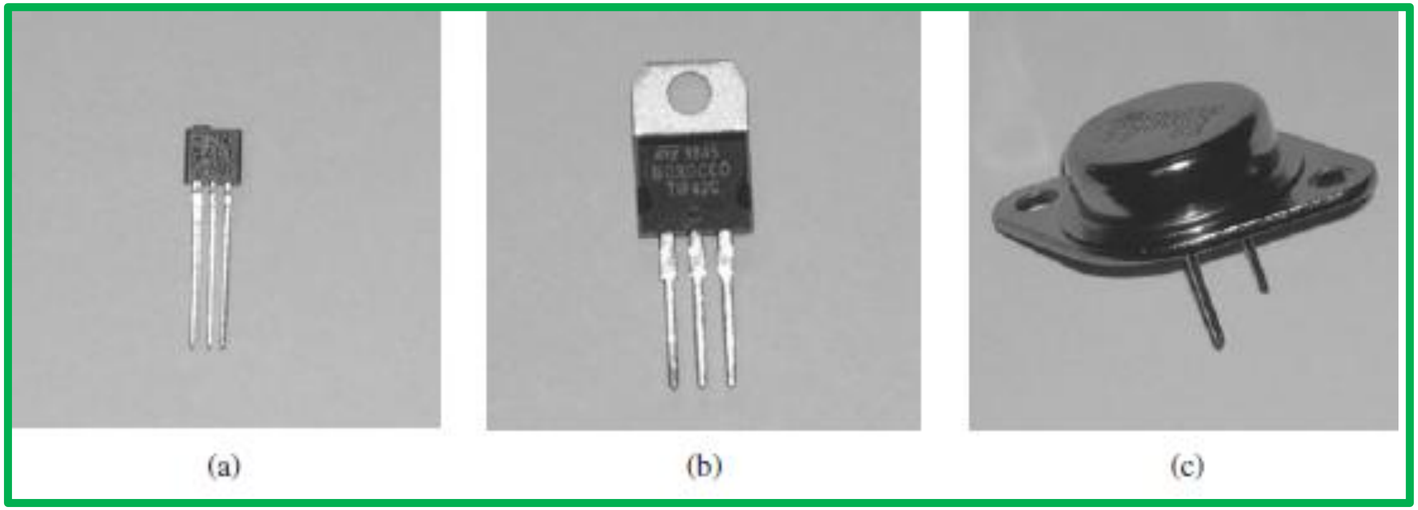


Figure 18 General-purpose or switching transistors (a) low power; (b) medium power; (c) medium to high power.

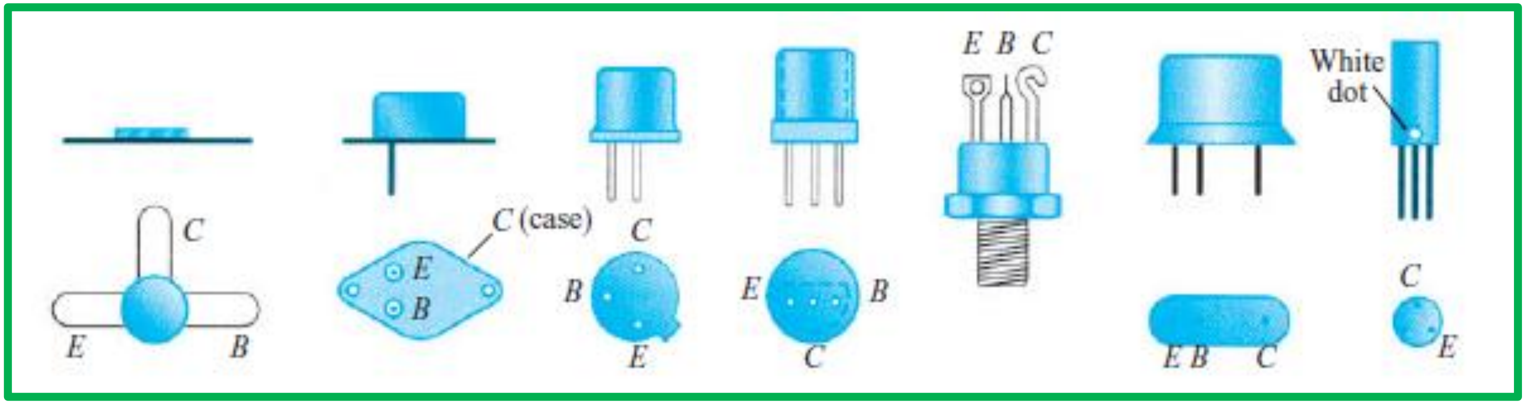


Figure 19 Transistor terminal identification.