EEE 3571 Electronic Engineering I

Lecture 4: DC Biasing of BJTs

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Dr. Daliso Banda

daliso.banda@unza.zm

Department of Electrical & Electronic Engineering, School of Engineering, University of Zambia

References

Our main reference text books in this course are

[1] Neil S., Electronics: A Systems Approach, 4th edition, 2009, Pearson Education Limited, ISBN 978-0-273-71918-2.

[2] Boylestad R. L., Nashelsky L., Electronic Devices and Circuit Theory, 11th Ed, 2013, Prentice-Hall, ISBN 978-0-13-262226-4.

[3] Smith R. J., Dorf R. C., Circuits Devices and Systems, 5th Ed., 2004, John Wiley, ISBN ISBN 9971-51-172-X.

However, feel free to use pretty much any additional text which you might find relevant to our course.

Learning Objectives

At the end of the lecture 4 on DC biasing of BJTs, you ought to:

1. Be able to determine the dc levels for the variety of BJT configurations.
2. Understand how to measure important voltage levels for a BJT configuration and determine if the network is operating properly.
3. Become aware of the saturation and cutoff conditions of a BJT network.
4. Be able to perform a load-line analysis of the most common BJT configurations.
5. Become acquainted with the design process for BJT amplifiers.
6. Understand the basic operation of transistor switching networks.
7. Begin to understand the troubleshooting process as applied to BJT networks.
8. Develop a sense for the stability factors of a BJT configuration and how they affect it operation due to changes in specific characteristics and environment.

4.1 Introduction

- The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system.
- In transistor networks, any increase in ac voltage, current, or power is the result of a transfer of energy from the applied dc supplies.
- The superposition theorem is used to determine dc and ac responses separately, so that their summation yields the total response.
- In design or synthesis, once the desired dc current and voltage levels have been defined, a network must be constructed that will establish the desired operating point.
- The analysis will chiefly exploit the following basic relationships:

$$V_{BE} \cong 0.7\,\text{V} \qquad [4.1]$$

$$I_E = (\beta + 1) I_B \cong I_C \qquad [4.2]$$

$$I_C = \beta I_B \qquad [4.3]$$

4.2 Operating Point

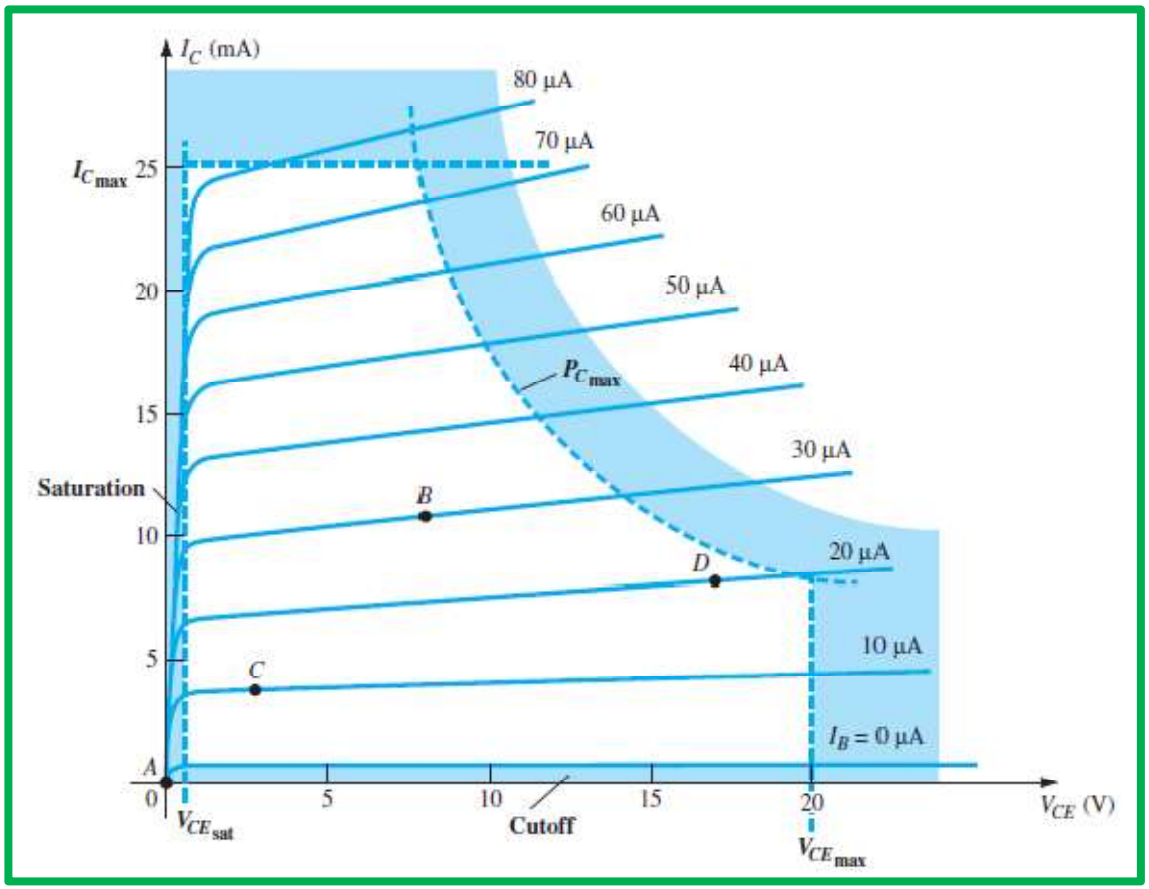


Figure 4.1: Various operating points within the limits of operation of a transistor.

- For transistor amplifiers the applied biasing dc voltages establish a fixed level of current and voltage on the characteristics for small-signal amplification.
- The fixed point established is called the quiescent point (Q-point).
- The BJT device biased to operate outside the maximum limits culminates in shortened lifetime or destruction of the device.

4.3 Fixed-Bias Configuration

- Shown is the simplest *npn* transistor dc bias configuration.

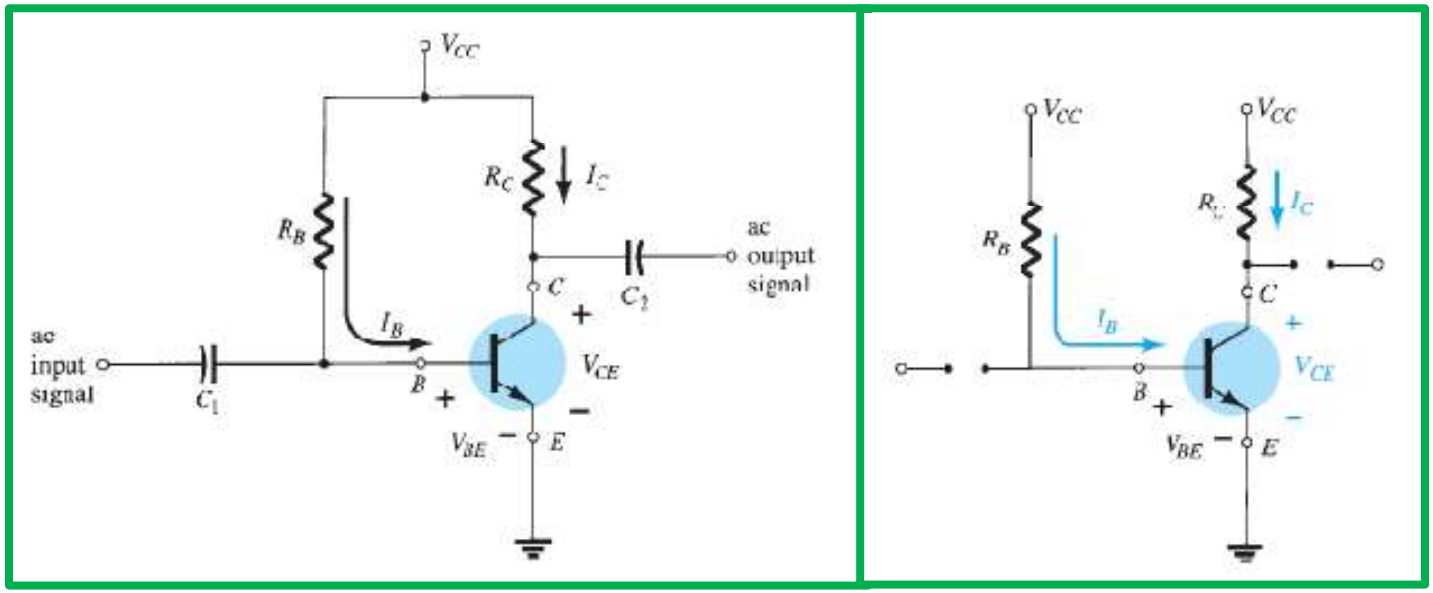


Figure 4.2: (a) Fixed-bias circuit; (b) Dc equivalent of Fig. 4.2.

- For dc analysis the network is isolated from ac levels by replacing the capacitors with open circuits.
- It follows from capacitive reactance, given $f = 0\,\text{Hz}$, yields

$$X_C = 1/2\pi fC = 1/2\pi(0)C = \infty\,\Omega$$

4.3 Fixed-Bias Configuration Cont'd

Forward Bias of Base-Emitter

- Consider first the base-emitter circuit loop of Fig. 4.3. Applying KVL yields

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

- Solving the equation for I_B yields

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \qquad [4.4]$$

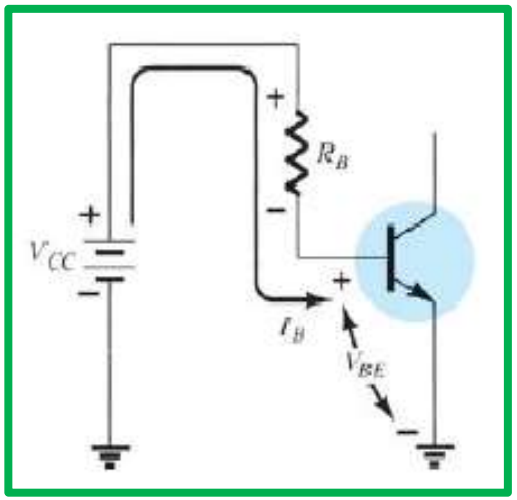


Figure 4.3: Base-emitter loop.

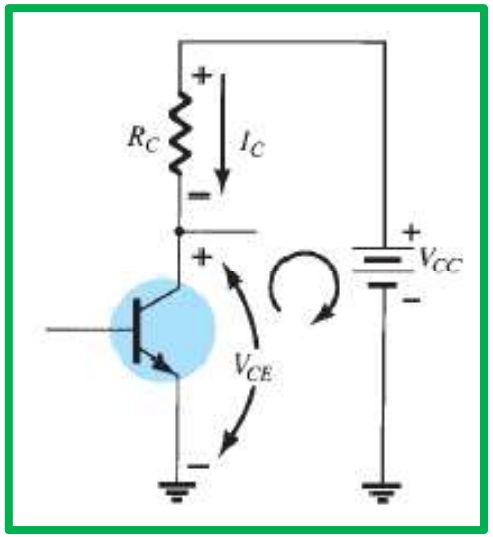


Figure 4.4: Collector-emitter loop.

Collector-Emitter Loop

- Recall that,

$$I_C = \beta I_B \qquad [4.5]$$

- Note that changing R_C to any level will not affect the level of I_B or I_C so long this is with active region.

4.3 Fixed-Bias Configuration Cont'd

- Applying KVL to Fig. 4.4 yields

$$V_{CE} + I_C R_C - V_{CC} = 0 \; ; \; \Rightarrow \quad \boxed{V_{CE} = V_{CC} - I_C R_C} \qquad [4.6]$$

- Vividly, V_{CE} in fixed bias configuration is the supply voltage less the drop across R_C.
- Recall that, $\boxed{V_{CE} = V_C - V_E}$ [4.7]
- Since $V_E = 0\,\text{V}$, we have $\boxed{V_{CE} = V_C}$ [4.8]
- Furthermore, $\boxed{V_{BE} = V_B - V_E}$ [4.9]
- Since $V_E = 0\,\text{V}$, we have $\boxed{V_{BE} = V_B}$ [4.10]

Example 4.1 Fixed-Bias Configuration

❑ Determine the following for the fixed-bias configuration of Fig. 4.5.

a) I_{B_Q} and I_{C_Q}.

b) V_{CE_Q}.

c) V_B and V_C.

d) V_{BC}.

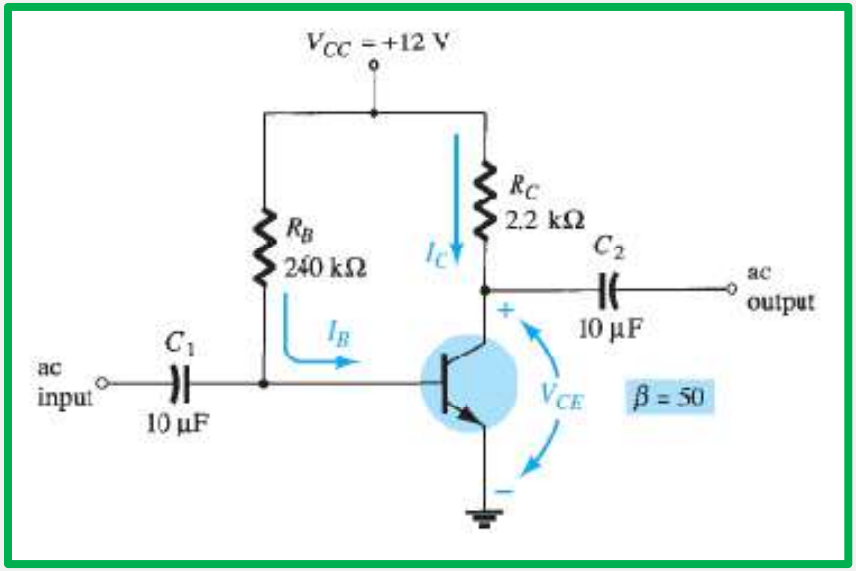


Figure 4.5: DC fixed-bias circuit for Ex. 4.1.

[Solution]

a) Eq. [4.4]: $$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\,\text{V} - 0.7\,\text{V}}{240\,\text{k}\Omega};$$

$$I_{B_Q} = 47.08\,\mu\text{A}$$

Eq. [4.5]: $$I_{C_Q} = \beta I_{B_Q} = (50)(47.08\,\mu\text{A});$$

$$I_{C_Q} = 2.35\,\text{mA}$$

b) Eq. [4.6]: $$V_{CE_Q} = V_{CC} - I_C R_C;$$

$$V_{CE_Q} = 12V - (2.35\,\text{mA})(2.2\,\text{k}\Omega);$$

$$V_{C_Q} = 6.83\,\text{V}$$

Example 4.1 Fixed-Bias Configuration Cont'd

b) Eqs. [4.10] and [4.8]: $V_B = V_{BE} = 0.7\,\text{V}$

$V_C = V_{CE} = 6.83\,\text{V}$

c) Using double-subscript notation yields

$$V_{BC} = V_B - V_C = 0.7\,\text{V} - 6.83\,\text{V}; \quad V_{BC} = -6.13\,\text{V}$$

d) The negative sign reveals that the junction is reverse-biased, as it should be for linear amplification.

4.3 Fixed-Bias Configuration Cont'd

Transistor Saturation

- The term saturation is applied to any system where levels have reached their maximum values.
- For a transistor operating in the saturation region, the current is a maximum value for the particular design.

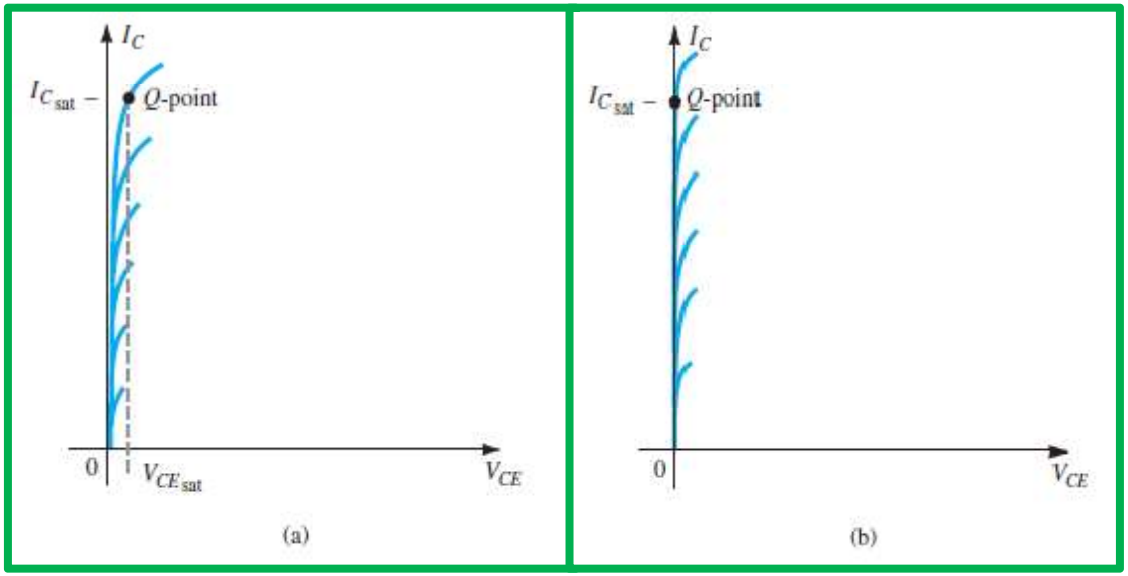


Figure 4.6: Saturation regions: (a) actual; (b) approximate.

- Fig. 4.6a depicts an operating point in the saturation region.
- Note that in this region the characteristic curves join and $V_{CE} \leq V_{CE_{sat}}$.
- Let Fig. 4.6a be approximated by Fig. 4.6b. Clearly, the current is relatively high and assume $V_{CE} = 0\ \text{V}$.

4.3 Fixed-Bias Configuration Cont'd

- Exploiting Ohm's law, we determine the resistance between collector and emitter terminals as follows:

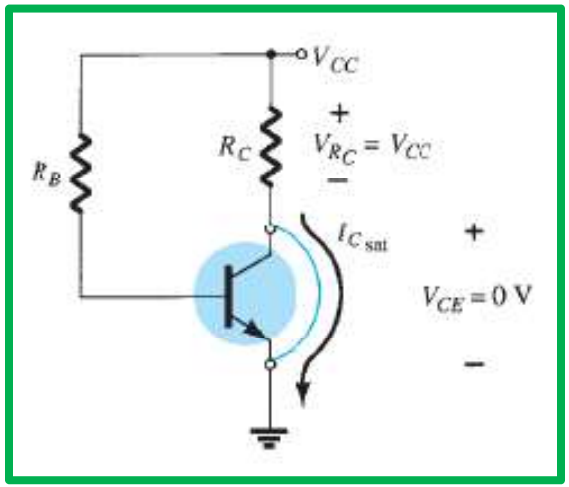


Figure 4.7: Determining $I_{C_{sat}}$ for the fixed-bias configuration.

$$R_{CE} = \frac{V_{CE}}{I_C} = \frac{0\text{ V}}{I_{C_{sat}}} = 0\ \Omega$$

- For the future, to know the approximate maximum collector current (saturation level) for a particular design, simply insert a short-circuit equivalent between collector and emitter of the BJT and calculate $I_{C_{sat}}$.
- For the fixed-bias configuration of Fig. 4.7, having applied the short-circuit, it follows that

$$I_{C,\text{sat}} = \frac{V_{CC}}{R_C} \qquad [4.11]$$

4.3 Fixed-Bias Configuration Cont'd

Load-Line Analysis

- The characteristics of the BJT are superimposed on a plot of the network equation define by the same axis parameters called dc load-line.

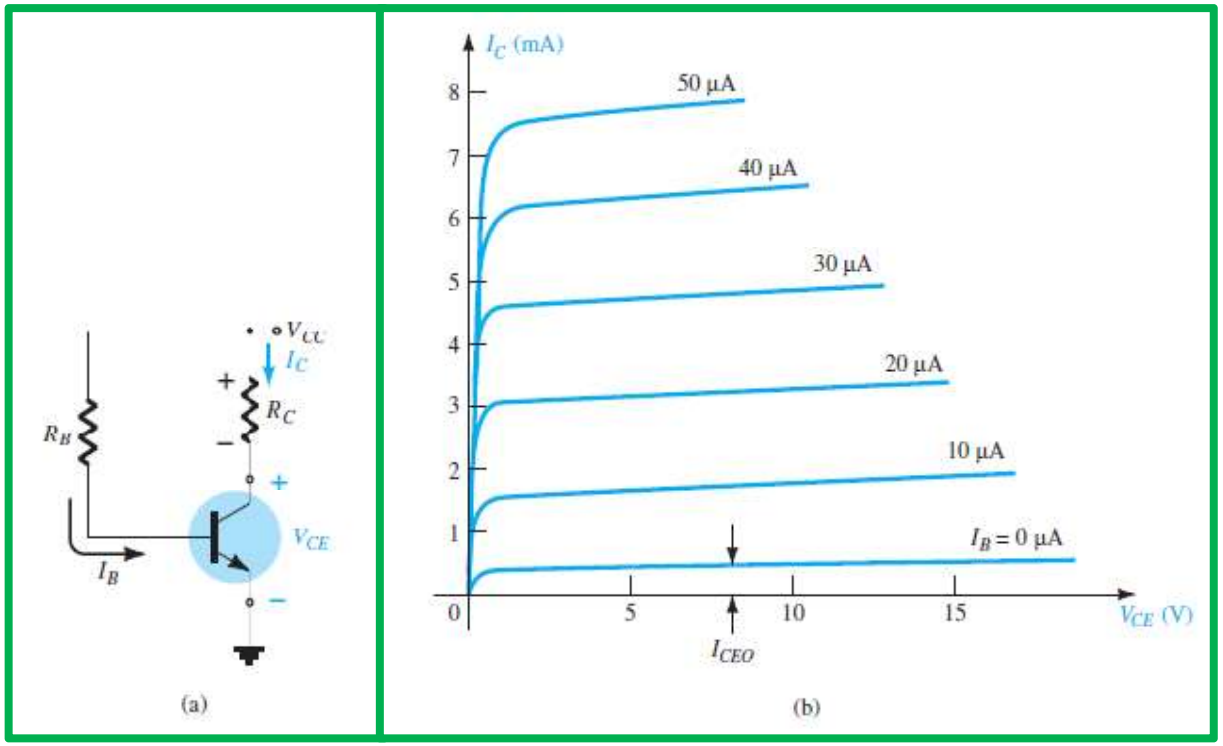


Figure 4.8: Load-line analysis: (a) the network; (b) the device characteristics..

- From Fig. 4.8a an output equation that relates I_C and V_{CE} is given by

$$V_{CE} = V_{CC} - I_C R_C \quad \textbf{[4.12]}$$

- Notice that the load resistor R_C determines the slope of the load-line.

4.3 Fixed-Bias Configuration Cont'd

- Co-plotting the load-line and output characteristic is aided by the fact that each case relates I_C and V_{CE} .

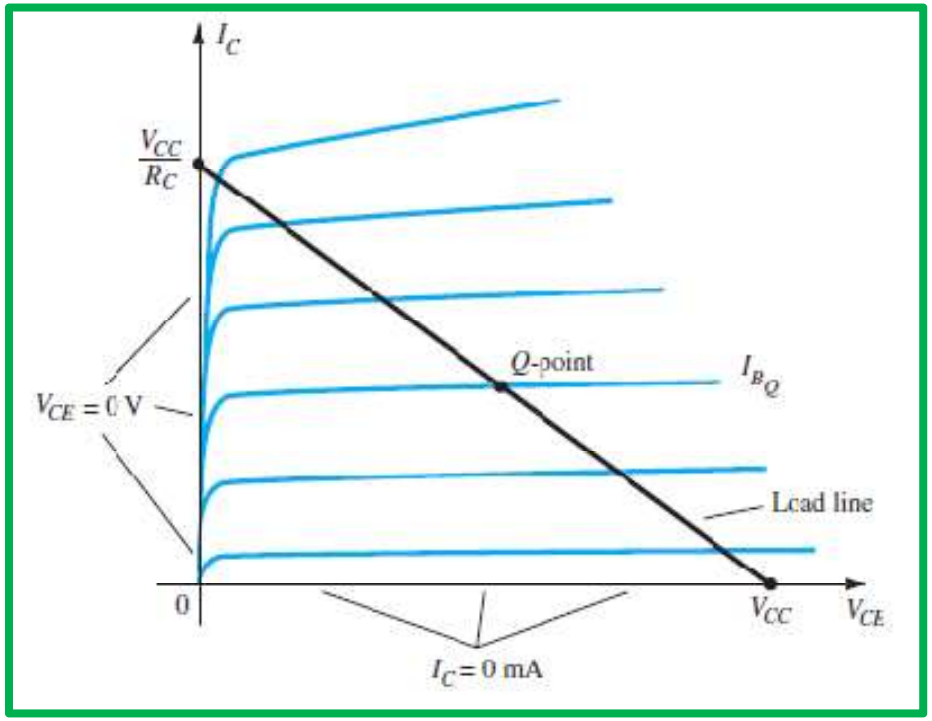


Figure 4.9: Fixed-bias load line.

- Let $I_C = 0\,\text{mA}$, it follows that

$$V_{CE} = V_{CC} - (0)R_C \;;$$

$$V_{CE} = V_{CC}\big|_{I_C = 0\,\text{mA}} \qquad [4.13]$$

- Furthermore, let $V_{CE} = 0\,\text{V}$ so that,

$$0 = V_{CC} - I_C R_C \;;$$

$$I_C = \frac{V_{CC}}{R_C}\bigg|_{V_{CE} = 0\,\text{V}} \qquad [4.14]$$

- The point of intersection is *Q*uiescent point (*Q*-point).

4.3 Fixed-Bias Configuration Cont'd

- The level of I_B is changed by varying the value of R_B the effect of which is depicted in Fig. 4.10.

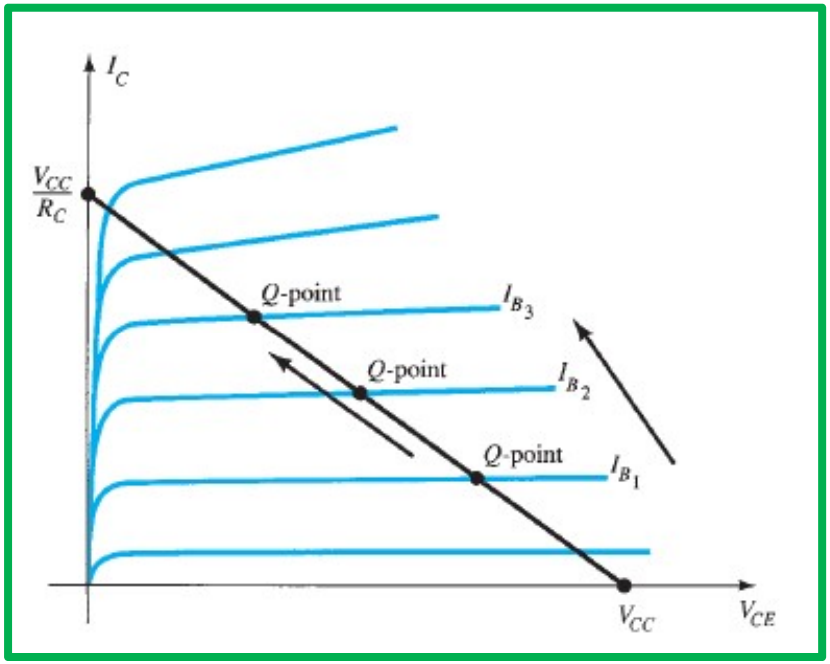


Figure 4.10: Movement of *Q*-point with increasing level of I_B .

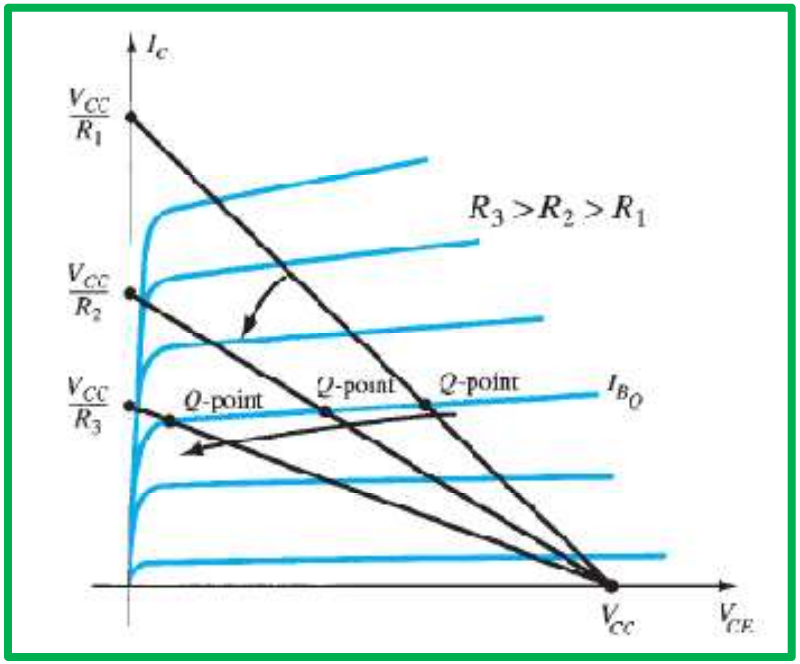


Figure 4.11: Effect of an increasing level of R_C on the load line and the *Q*-point.

- Holding V_{CC} constant, if R_C is increased, the load line will shift (less steep slope) as shown in Fig. 4.11.

4.3 Fixed-Bias Configuration Cont'd

- Holding R_C constant, if V_{CC} is decreased, the load line will shift (same slope) as shown in Fig. 4.12.

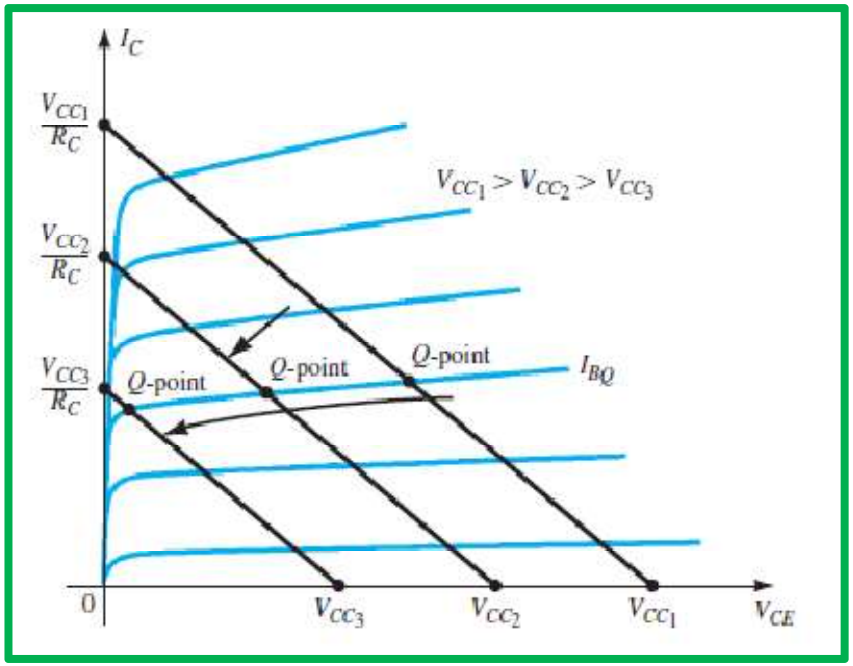


Figure 4.12: Effect of lower values of V_{CC} on the load line and the *Q*-point.

Example 4.2 Fixed-Bias Configuration

- Given the load line of Fig. 4.13 and the defined Q-point, determine the required values of V_{CC} , R_C , and R_B for a fixed-bias configuration.

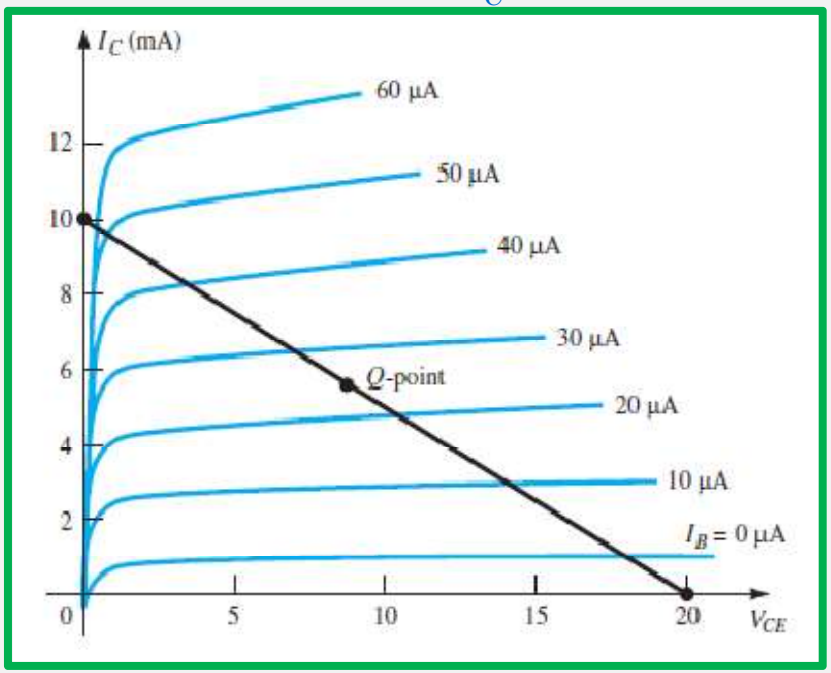


Figure 4.13: Example 4.2.

[Solution]

- From Fig. 4.13,

$$V_{CE} = V_{CC} = \mathbf{20\,V}\,; \quad \text{at} \quad I_C = 0\,\text{mA}$$

$$I_C = \frac{V_{CC}}{R_C}\,; \quad \text{at} \quad V_{CE} = \mathbf{0\,V}$$

- Thus, we have

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\,\text{V}}{10\,\text{mA}} = \mathbf{2\,k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}\,;$$

- It follows that,

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\,\text{V} - 0.7\,\text{V}}{25\,\mu\text{A}} = \mathbf{772\,k\Omega}$$

4.4 Emitter-Bias Configuration

- The emitter resistor in Fig. 4.14 helps to improve the stability level over that of fixed-bias configuration.
- The mores stable a configuration, the less its response will change due to undesirable changes in temperature and parameter variations.
- The DC equivalent circuit for Fig. 4.14 is shown in Fig. 4.15.

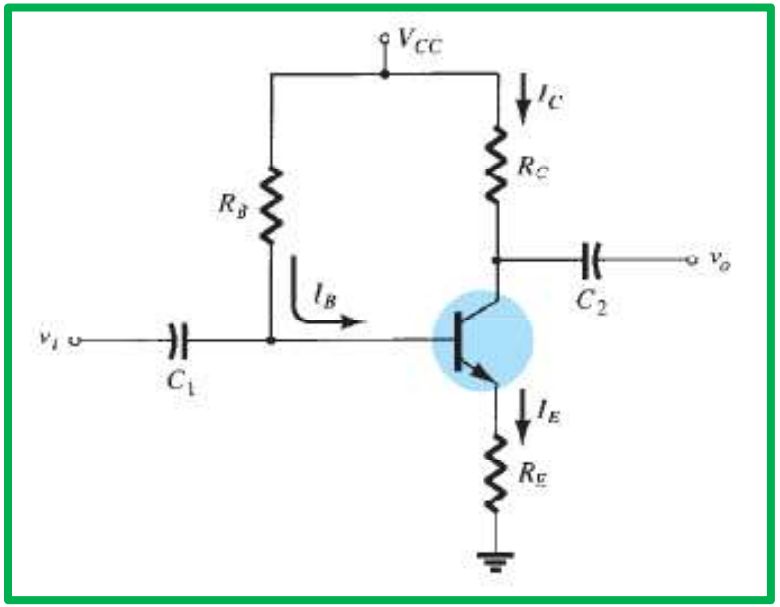


Figure 4.14: BJT bias circuit with emitter resistor.

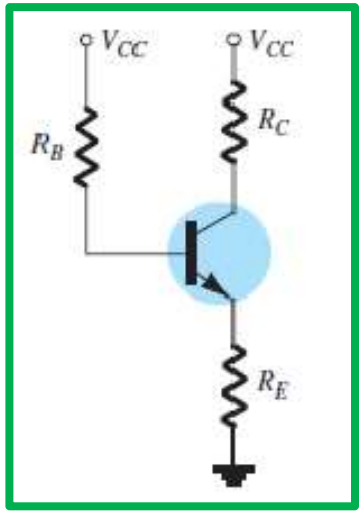


Figure 4.15: DC equivalent of Fig. 4.14.

4.4 Emitter-Bias Configuration Cont'd

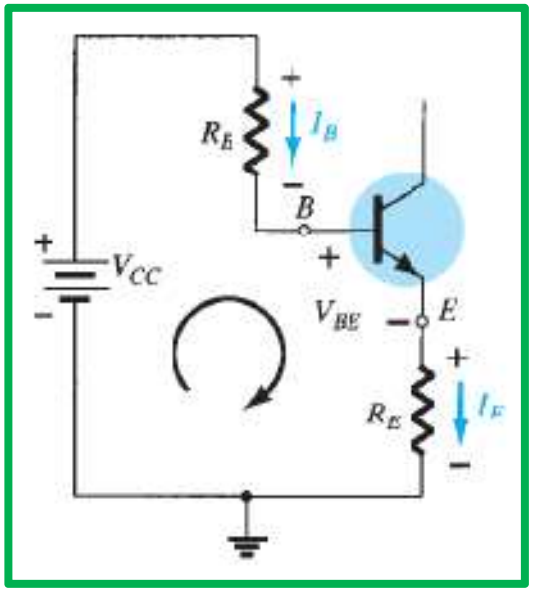


Figure 4.16: Base-emitter loop.

Base-Emitter Loop

- The circuit of Fig. 4.15 is redrawn in Fig. 4.16. Exploiting KVL yields

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \qquad [4.15]$$

- Recall that, $I_E = (\beta + 1) I_B$ [4.16]

- Substituting for I_E in Eq. [4.15] yields,

$$+V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

- It follows that,

$$-I_B \left(R_B + (\beta + 1) R_E\right) + V_{CC} - V_{BE} = 0 \;;$$

$$\Rightarrow \quad I_B \left(R_B + (\beta + 1) R_E\right) = V_{CC} - V_{BE} \;;$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} \qquad [4.17]$$

4.4 Emitter-Bias Configuration Cont'd

- Notice the difference between Eq. [4.17] and that obtained for the fixed-bias configuration is the term $(\beta+1)R_E$.

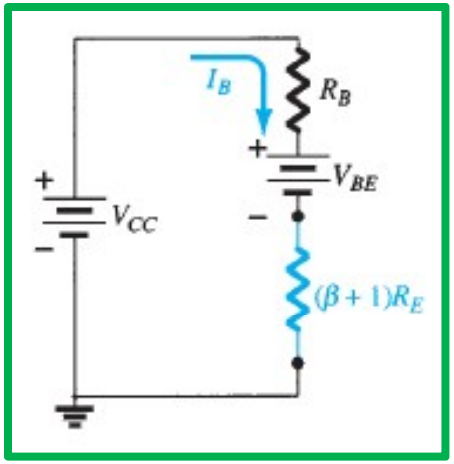


Figure 4.17: Network derived from Eq. [4.17].

- Eq. [4.17] is used to sketch a series network of Fig. 4.17.
- The resistor R_E is *reflected* back to the input base circuit by a factor $(\beta+1)$.
- In general, therefore, for the configuration of Fig. 4.18,

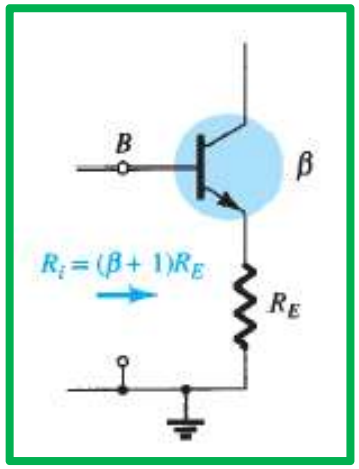


Figure 4.18: Reflected impedance level of R_E .

$$R_i = (\beta+1)R_E \qquad [4.18]$$

4.4 Emitter-Bias Configuration Cont'd

Collector-Emitter loop

- Applying KVL to the loop of Fig. 4.19 yields

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

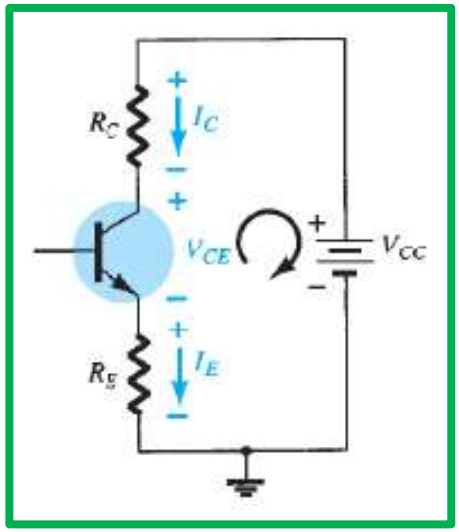


Figure 4.19: Collector-emitter loop.

- Substituting $I_E \cong I_C$ and grouping terms gives

$$V_{CE} - V_{CC} + I_C\left(R_C + R_E\right) = 0$$

- Thus,

$$V_{CE} = V_{CC} - I_C\left(R_C + R_E\right) \qquad [4.19]$$

- The single-subscript voltage V_E is the voltage from emitter to ground and is determined by

$$V_E = I_E R_E \qquad [4.20]$$

- The voltage from collector to ground is found using

$$V_{CE} = V_C - V_E \;;\quad V_C = V_{CE} + V_E \qquad [4.21]$$

- Thus,

$$V_C = V_{CC} - I_C R_C \qquad [4.22]$$

4.4 Emitter-Bias Configuration Cont'd

- The voltage at the base with respect to ground is obtained using Fig. 4.15 as

$$V_B = V_{CC} - I_B R_B \qquad [4.23]$$

- It follows that,

$$V_B = V_{BE} + V_E \qquad [4.24]$$

Example 4.3 Emitter-Bias Configuration

- For the emitter-bias network of Fig. 4.20, determine:

a) I_B.
b) I_C.
c) V_{CE}.
d) V_C.
e) V_E.
f) V_B.
g) V_{BC}

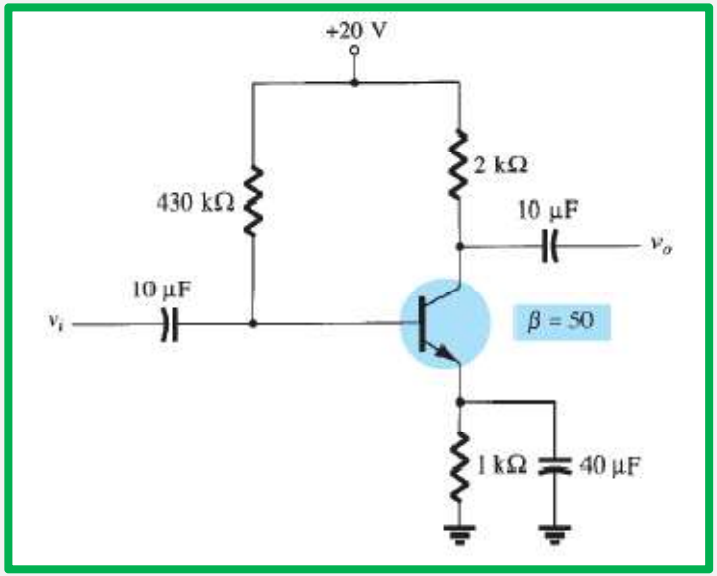


Figure 4.20: Emitter-stabilized circuit for Example 4.4

Example 4.3 Emitter-Bias Configuration Cont'd

[Solution]

a) Eq. [4.17]: $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\,\text{V} - 0.7\,\text{V}}{430\,\text{k}\Omega + (51)(1\,\text{k}\Omega)} = \frac{19.3\,\text{V}}{481\,\text{k}\Omega};$$

$$I_B = \mathbf{40.1\,\mu A}$$

b) $$I_C = \beta I_B = (50)(40.1\,\mu\text{A}); \qquad I_C \cong \mathbf{2.01\,mA}$$

c) Eq. [4.19]: $$V_{CE} = V_{CC} - I_C(R_C + R_E) = 20\,\text{V} - (2.01\,\text{mA})(2\,\text{k}\Omega + 1\,\text{k}\Omega);$$

$$V_C = 20\,\text{V} - 6.03\,\text{V} = \mathbf{13.97\,V}$$

d) $$V_C = V_{CC} - I_C R_C = 20\,\text{V} - (2.01\,\text{mA})(2\,\text{k}\Omega) = 20\,\text{V} - 4.02\,\text{V};$$

$$V_C = \mathbf{15.98\,V}$$

e) $$V_E = V_C - V_{CE} = 15.98\,\text{V} - 13.97\,\text{V} = \mathbf{2.01\,V}$$

Alternatively, $$V_C = I_E R_E \cong I_C R_E = (2.01\,\text{mA})(1\,\text{k}\Omega) = \mathbf{2.01\,V}$$

f) $$V_B = V_{BE} + V_E = 0.7\,\text{V} + 2.01\,\text{V} = \mathbf{2.71\,V}$$

Example 4.3 Emitter-Bias Configuration Cont'd

f) $V_{BC} = V_B - V_C = 2.71\,\text{V} - 15.98\,\text{V} = \mathbf{-13.27\,V}$ (reverse-biased as required)

Improved Bias Stability

- The emitter resistor added to the dc bias of the BJT provides improved stability in that, the dc bias currents and voltages remain closer to where they were set by circuit when outside conditions, such as temperature and transistor beta, change.

Saturation Level

- The collector saturation level or maximum collector current for an emitter-bias design is determined by applying a short-circuit in Fig. 4.21. It follows that,

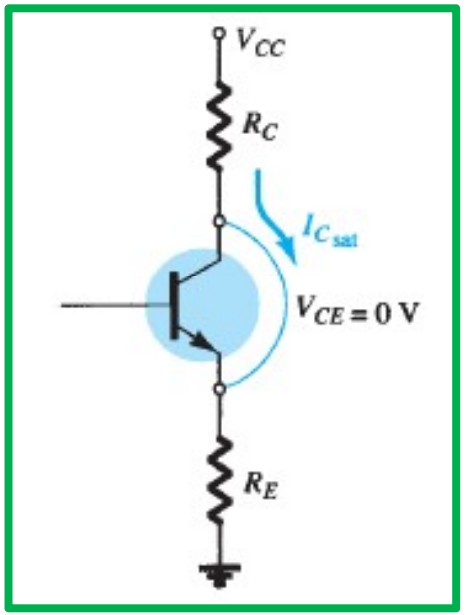


Figure 4.21: Determining $I_{C_{sat}}$ for the emitter-stabilized bias circuit.

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E} \qquad [4.25]$$

4.4 Emitter-Bias Configuration Cont'd

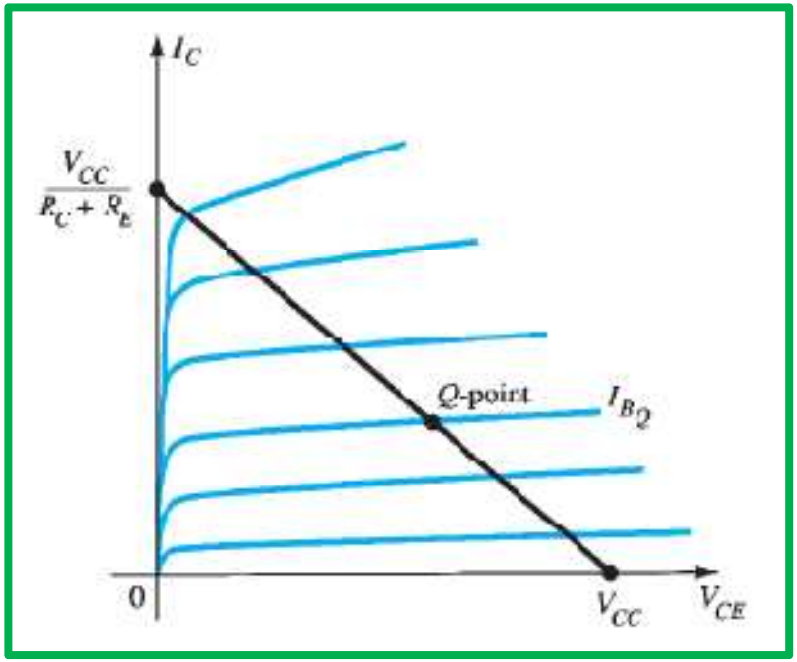


Figure 4.22: Load line for the emitter-bias configuration.

Load-Line Analysis

- The load-line analysis of the emitter-bias network is only slightly different from that of fixed-bias design.
- Thus, the collector-emitter loop equation that defines the load line is

$$V_{CE} = V_{CC} - I_C\left(R_C + R_E\right)$$

- Let $I_C = 0\ \text{mA}$, it follows that

$$V_{CE} = V_{CC} - (0)\left(R_C + R_E\right);$$

$$V_{CE} = V_{CC}\big|_{I_C = 0\ \text{mA}} \qquad [4.26]$$

- Furthermore, let $V_{CE} = 0\ \text{V}$ so that,

$$0 = V_{CC} - I_C\left(R_C + R_E\right);$$

$$I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE} = 0\ \text{V}} \qquad [4.27]$$

4.5 Voltage-Divider Bias Configuration

- Thus far, in the bias designs we have discussed the bias current I_{C_Q} and voltage V_{CE_Q} were a function of the current gain β of the transistor.
- However, beta is temperature sensitive, especially for silicon transistors, thus its actual value is usually not well defined.
- To mitigate this beta dependence problem the voltage-divider bias design of Fig. 4.23 can be used.

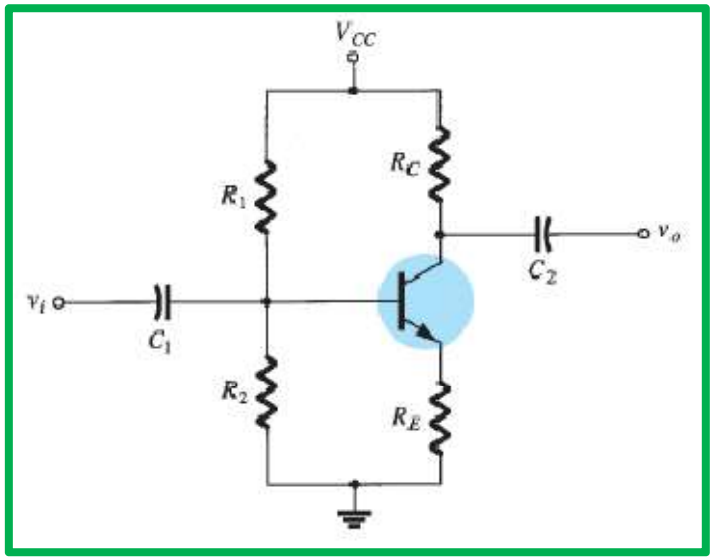


Figure 4.23: Voltage-divider bias configuration.

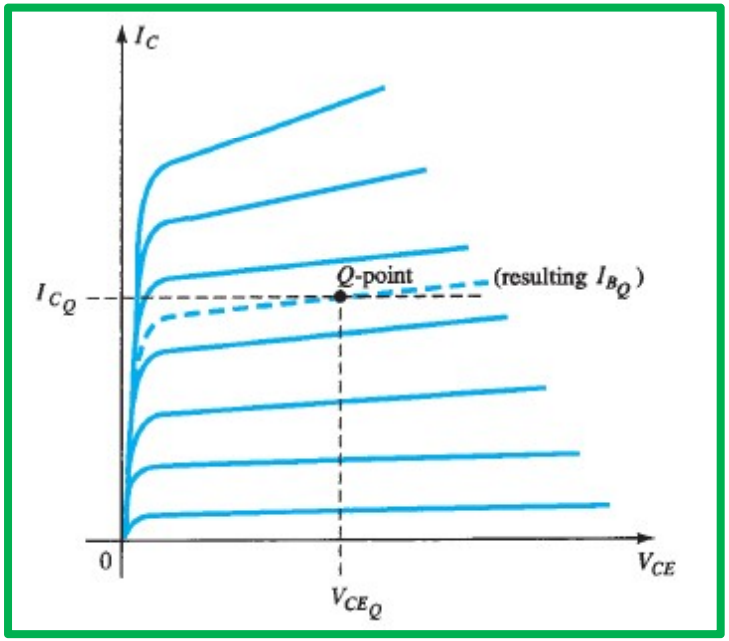


Figure 4.24: Defining the *Q*-point for the voltage-divider bias configuration.

4.5 Voltage-Divider Bias Configuration Cont'd

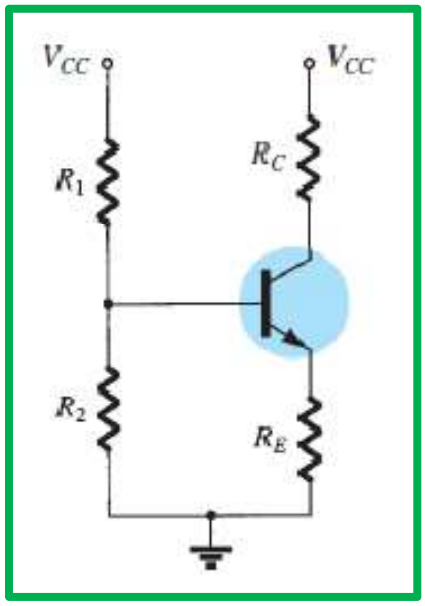


Figure 4.25: DC components of the voltage-divider bias design.

Exact Analysis

- For dc analysis Fig. 4.23 is redrawn as shown in Fig. 4.25. The input side is further redrawn in Fig. 4.26.
- The Thevenin equivalent circuit to the left of the base terminal is found as follows:
- To find R_{Th} , short circuit the voltage source so that,

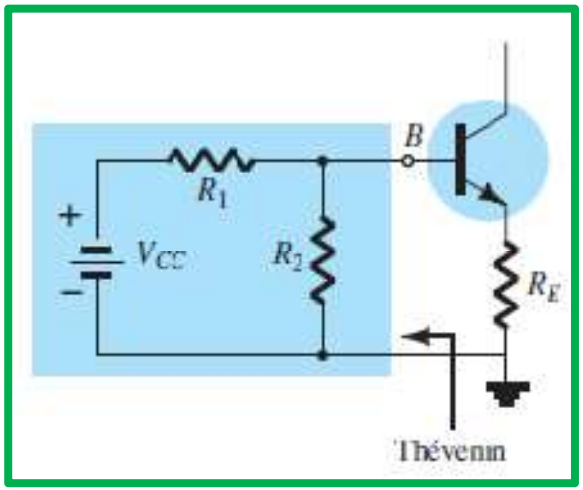


Figure 4.26: Redrawing the input side of the network of Fig. 4.25.

$$R_{Th} = R_1 \| R_2 \qquad [4.28]$$

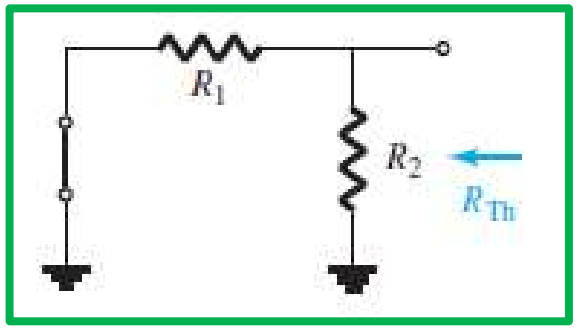


Figure 4.27: Determining R_{Th} .

4.5 Voltage-Divider Bias Configuration Cont'd

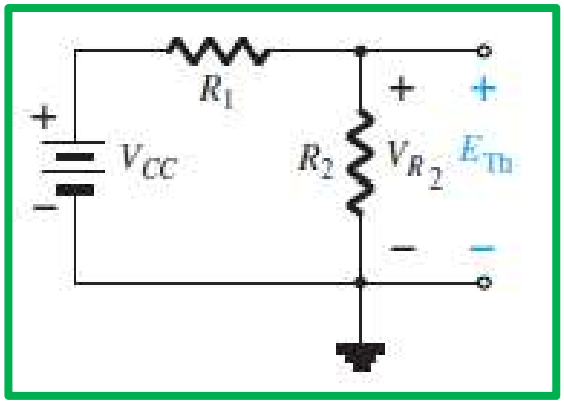


Figure 4.28: Determining E_{Th} .

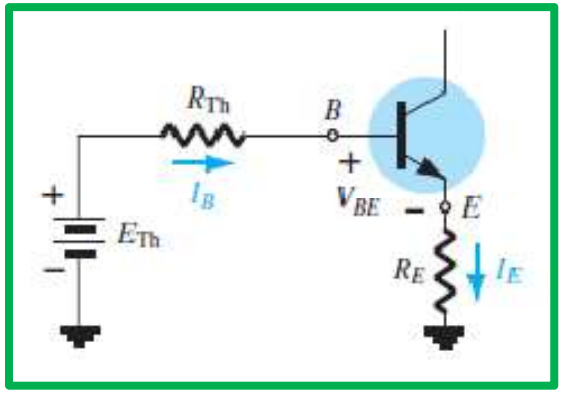


Figure 4.29: Inserting the Thevenin equivalent circuit.

- The open-circuit Thevenin voltage E_{Th} is determined with voltage source V_{CC} returned to the network, see Fig. 4.28. Applying voltage divider rule yields

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2} \qquad [4.29]$$

- Thus, the Thevenin network is redrawn in Fig. 4.34, and I_{B_Q} can be determined by applying KVL, that is

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0;$$

- Substituting $I_E = (\beta + 1) I_B$ yields,

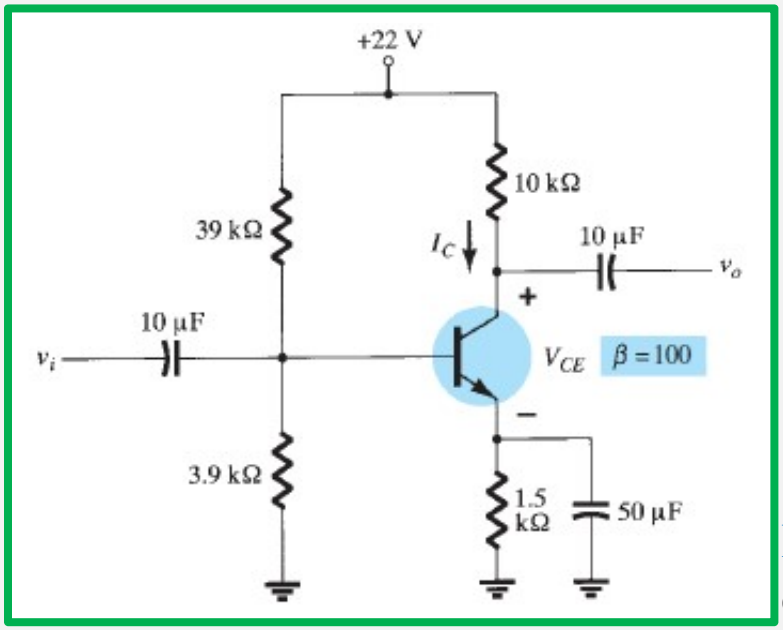
$$I_B = V_{R_2} = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E} \qquad [4.30]$$

4.5 Voltage-Divider Bias Configuration Cont'd

- Once I_B is known, the remaining quantities of the network can be found in the same manner as for the emitter-bias configuration. That is,

$$V_{CE} = V_{CC} - I_C\left(R_C + R_E\right) \qquad [4.31]$$

Example 4.4 Voltage-Divider Bias Configuration



- Determine the dc bias voltage V_{CE} and the current I_C for the voltage divider configuration of Fig. 4.30.

[Solution] Eq. [4.28]:

$$R_{Th} = R_1 \| R_2 = \frac{(39\,\text{k}\Omega)(3.9\,\text{k}\Omega)}{39\,\text{k}\Omega + 3.9\,\text{k}\Omega} = 3.55\,\text{k}\Omega$$

Figure 4.30: Beta-stabilized circuit for Example 4.4.

Example 4.4 Voltage-Divider Bias Configuration

Eq. [4.29]: $$E_{\text{Th}} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9\,\text{k}\Omega)(22\,\text{V})}{39\,\text{k}\Omega + 3.9\,\text{k}\Omega} = 2\,\text{V}$$

Eq. [4.30]: $$I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E} = \frac{2\,\text{V} - 0.7\,\text{V}}{3.55\,\text{k}\Omega + (101)(1.5\,\text{k}\Omega)} = 8.38\,\mu\text{A}$$

$$I_C = \beta I_B = (100)(8.38\,\mu\text{A}) = \mathbf{0.84\,mA}$$

Eq. [4.31]: $$V_{CE} = V_{CC} - I_C(R_C + R_E) = 22\,\text{V} - (0.84\,\text{mA})(10\,\text{k}\Omega + 1.5\,\text{k}\Omega);$$

$$V_{CE} = \mathbf{12.34\,V}$$

4.5 Voltage-Divider Bias Configuration Cont'd

Approximate Analysis

- The input section of the voltage-divider configuration can be represented by the circuit of Fig. 4.31.
- Recall the $R_i = (\beta + 1)R_E$ is the reflected resistance between base and emitter.
- Furthermore, $R_i \gg R_2$ such that $I_B \ll I_2$, thus $I_2 \cong I_1$.

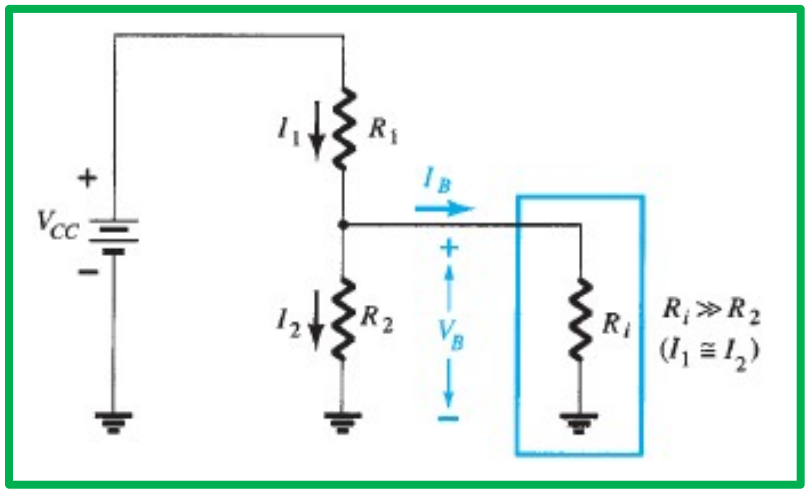


Figure 4.31: Partial-bias circuit for calculating the approximate base voltage V_B.

- With the approximation above the base voltage V_B is thus,

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} \qquad [4.32]$$

- Since $R_i = (\beta + 1)R_E \cong \beta R_E$ the condition to be met for the approximate analysis to hold is

$$\beta R_E \geq 10 R_2 \qquad [4.33]$$

4.5 Voltage-Divider Bias Configuration Cont'd

- Simply put, if the condition in Eq. [4.33] is met the approximate approach can be applied with a high degree of accuracy.
- Once V_B is determined, the level of V_E can be calculated from

$$V_E = V_B - V_{BE} \qquad [4.34]$$

- The emitter current can be determined from

$$I_E = \frac{V_E}{R_E} \qquad [4.35]$$

- It follows also that

$$I_{C_Q} \cong I_E \qquad [4.36]$$

- The collector-emitter voltage is determined by

$$V_{CE} = V_{CC} - I_C R_C + I_E R_E \ ;$$

- But $I_E \cong I_C$, thus

$$V_{CE_Q} = V_{CC} - I_C (R_C + R_E) \qquad [4.37]$$

- Note: the determination of I_{C_Q} and V_{CE_Q} is independent of β .

Example 4.5 Voltage-Divider Bias Configuration

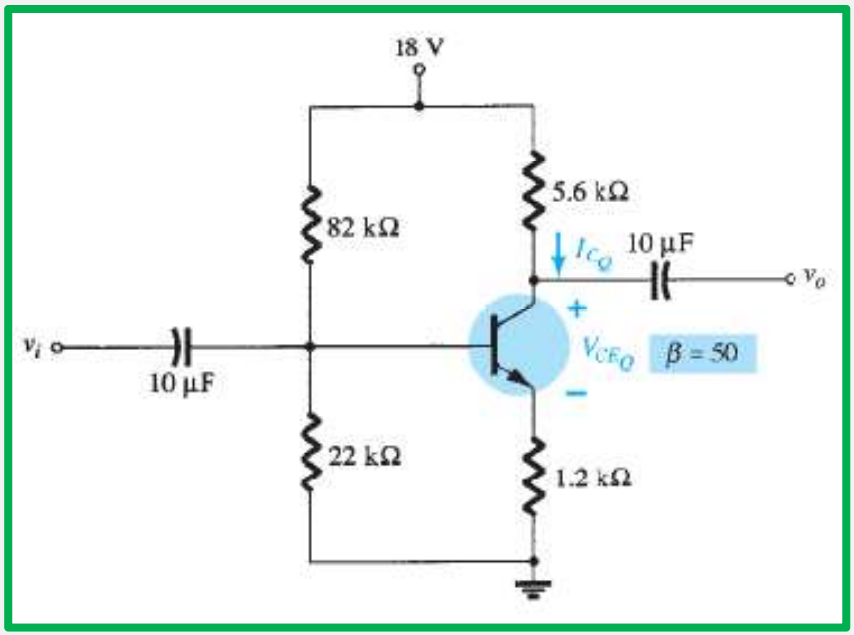


Figure 4.32: Voltage-divider configuration for Example 4.5.

- Determine the levels of I_{C_Q} and V_{CE_Q} for the voltage-divider configuration of Fig. 4.32 using the exact and approximate techniques and compare solutions.
- In this case, the conditions of Eq. [4.33] will not be satisfied and the results will reveal the difference in solution if the criterion of Eq. [4.33] is ignored.

[Solution]

- **Exact analysis**: Eq. [4.33]: $\beta R_E \geq 10R_2$

$$\Rightarrow (50)(1.2\text{k}\Omega) \geq 10(22\text{k}\Omega); \quad 60\text{k}\Omega \text{ Not greater or equal to } 220\text{k}\Omega$$

$$R_{\text{Th}} = R_1 \| R_2 = 82\text{k}\Omega \| 22\text{k}\Omega = 17.35\text{k}\Omega$$

Example 4.5 Voltage-Divider Bias Configuration Cont'd

$$E_{\text{Th}} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{22\,\text{k}\Omega(18\,\text{V})}{82\,\text{k}\Omega + 22\,\text{k}\Omega} = 3.81\,\text{V}$$

$$I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E} = \frac{3.81V - 0.7V}{17.35\,\text{k}\Omega + (51)(1.2\,\text{k}\Omega)} = \frac{3.11\,\text{V}}{78.55\,\text{k}\Omega} = 39.6\,\mu\text{A}$$

$$I_{C_Q} = \beta I_B = (50)(39.6\,\mu\text{A}) \; ; \qquad \boxed{I_{C_Q} = 1.98\,\text{mA}}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E) = 18\,\text{V} - (1.98\,\text{mA})(5.6\,\text{k}\Omega + 1.2\,\text{k}\Omega);$$

$$\boxed{V_{CE_Q} = 4.54\,\text{V}}$$

- **Approximate analysis**: $V_B = E_{\text{Th}} = 3.81\,\text{V}$

$$V_E = V_B - V_{BE} = 3.81\,\text{V} - 0.7\,\text{V} = 3.11\,\text{V}$$

$$I_{C_Q} \cong I_E = \frac{V_E}{R_E} = \frac{3.11\,\text{V}}{1.2\,\text{k}\Omega} \; ; \qquad \boxed{I_{C_Q} = 2.59\,\text{mA}}$$

Example 4.5 Voltage-Divider Bias Configuration Cont'd

$$V_{CE_Q} = V_{CC} - I_C\left(R_C + R_E\right) = 18\,\text{V} - \left(2.59\,\text{mA}\right)\left(5.6\,\text{k}\Omega + 1.2\,\text{k}\Omega\right);$$

$$V_{CE_Q} = 3.88\,\text{V}$$

Comparing the exact and approximate approaches.

	I_{C_Q} (mA)	V_{CE_Q} (V)
Exact	1.98	4.54
Approximate	2.59	3.88

Transistor Saturation

- The output collector-emitter circuit for the voltage-divider configuration has the same appearance as the emitter-biased circuit. Thus, the resulting equation for saturation current given that $V_{CE} = 0\,\text{V}$ is

$$I_{C_{\text{sat}}} = I_{C,\text{max}} = \frac{V_{CC}}{R_C + R_E} \qquad [4.38]$$

4.5 Voltage-Divider Bias Configuration Cont'd

Load-Line Analysis

- Similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration, i.e.,

$$V_{CE} = V_{CC}\big|_{I_C = 0\ \text{mA}} \qquad [4.39]$$

and

$$I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE} = 0\ \text{V}} \qquad [4.40]$$

- Notice that the level of I_B is determined by a different equation for the voltage-divider bias and the emitter-bias configurations.

4.6 Collector Feedback Configuration

- An improved level of stability is also obtained by introducing a feedback path from collector to base as shown in Fig. 4.33.

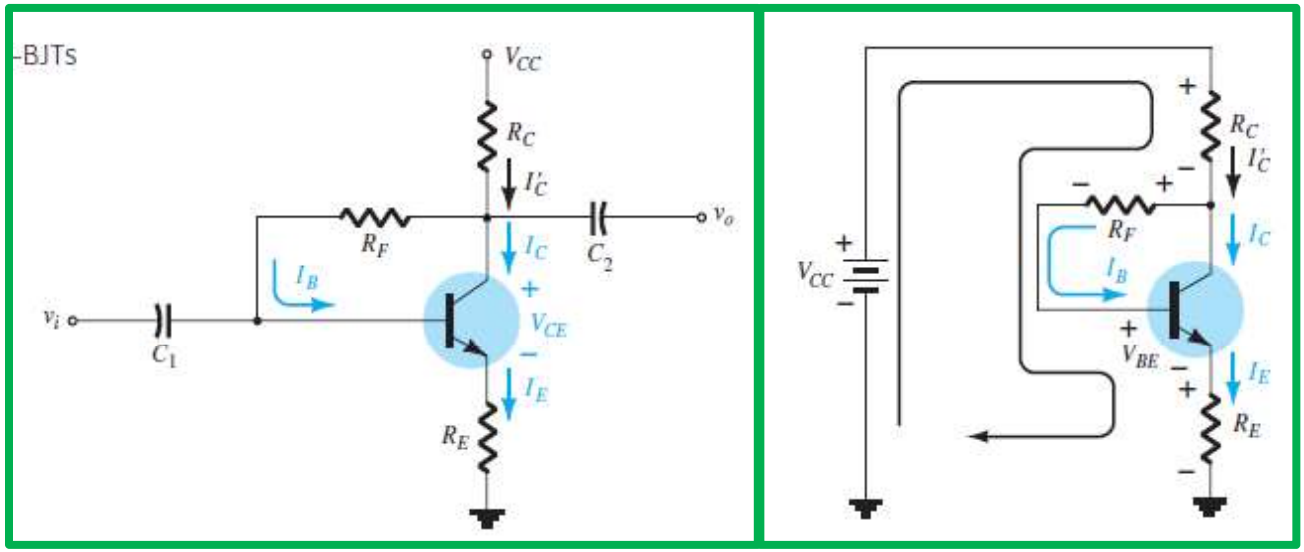


Figure 4.33: DC bias circuit with voltage feedback.

Figure 4.34: Base-emitter loop for the network of Fig. 4.33.

- The analysis is conducted as has been done previously.
- Perform base-emitter loop and apply the results to the collecter-emitter loop.

Base-Emitter Loop

- KVL yields: $V_{CC} - I'_C R_C - I_B R_F - V_{BE} - I_E R_E = 0$
- But, $I'_C = I_C + I_B$; thus substituting $I'_C \cong I_C = \beta I_B$ and $I_E \cong I_C$ gives

4.6 Collector Feedback Configuration Cont'd

$$V_{CC} - \beta I_B R_C - I_B R_F - V_{BE} - \beta I_B R_E = 0$$

$$\Rightarrow \; V_{CC} - V_{BE} - \beta I_B \left(R_C + R_E \right) - I_B R_F = 0 \; ;$$

- Solving for I_B yields

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta \left(R_C + R_E \right)} \qquad [4.41]$$

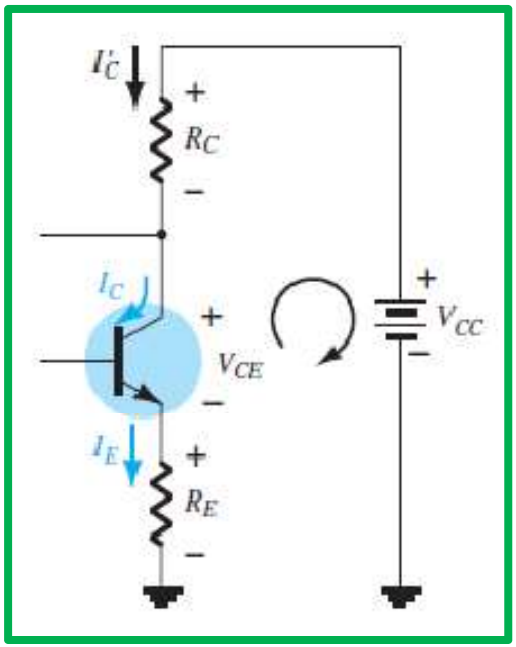


Figure 4.35: Collector-emitter loop for the network of Fig. 4.33.

Collector-Emitter Loop

- KVL applied to Fig. 4.35 yields:

$$I_E R_E + V_{CE} - I'_C R_C - V_{CC} = 0$$

- Since $I'_C \cong I_C$ and $I_E \cong I_C$, we have

$$V_{CE} = V_{CC} - I_C \left(R_C + R_E \right) \qquad [4.42]$$

- Exactly the as was obtained for the emitter-bias and voltage-divider bias configurations.

4.6 Collector Feedback Configuration Cont'd

Saturation Conditions

- By the approximation $I'_C = I_C$, we find that the equation for saturation current is the same as that of voltage-divider and emitter-bias configurations.

$$I_{C_{\text{sat}}} = I_{C,\max} = \frac{V_{CC}}{R_C + R_E} \qquad [4.43]$$

Load-Line Analysis

- Continuing to let $I'_C = I_C$ yields the same load line as was obtained for the last two configurations.

4.7 Emitter-Follower Configuration

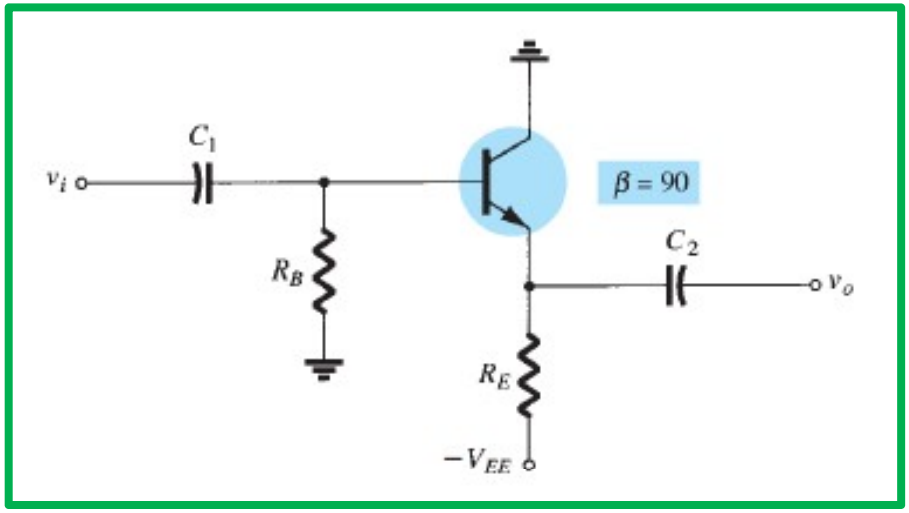


Figure 4.36: Common-collector (emitter-follower) configuration.

- Here the output is taken off the emitter terminal.

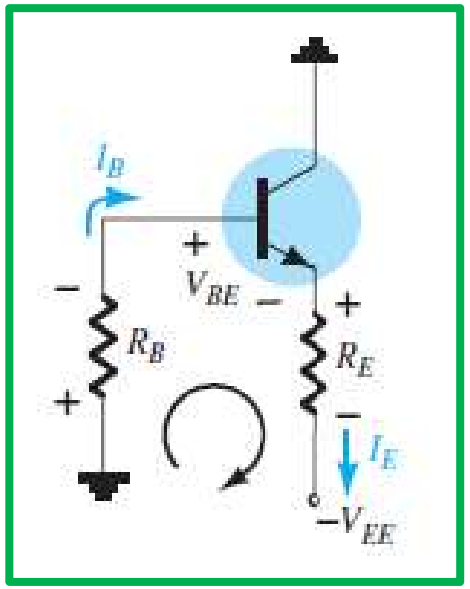


Figure 4.37: dc equivalent of Fig. 4.36.

- Applying Kirchhoff's voltage law to the input circuit yields

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0 \; ; \quad \text{but} \quad I_E = (\beta + 1) I_B \; ;$$

$$\Rightarrow \; I_B R_B + (\beta + 1) I_B R_E = V_{EE} - V_{BE} \; ; \qquad I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1) R_E} \qquad [4.44]$$

4.7 Emitter-Follower Configuration Cont'd

- For the output network, exploiting Kirchhoff's voltage law yields

$$-V_{CE} - I_E R_E + V_{EE} = 0 \; ; \; \Rightarrow \quad \boxed{V_{CE} = V_{EE} - I_E R_E} \qquad [4.45]$$

Example 4.6 Emitter-Follower Configuration

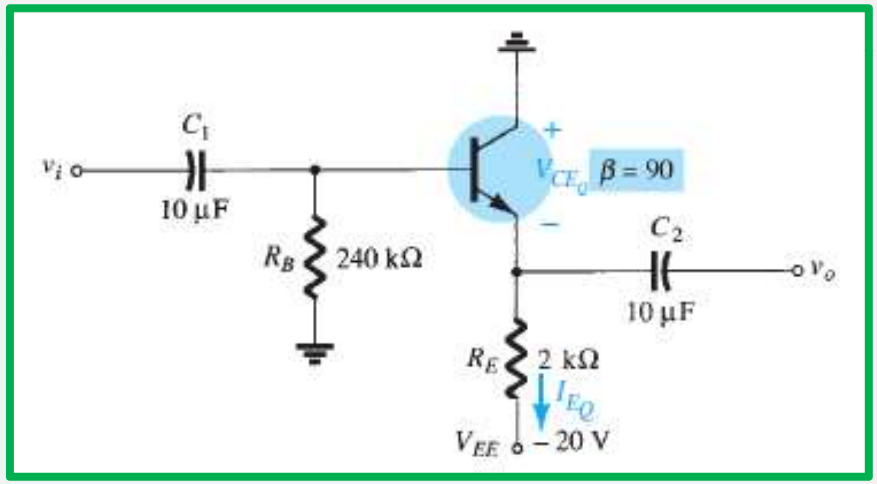


Figure 4.38: Example 4.6.

- Determine V_{CE_Q} and I_{E_Q} for the network of Fig. 4.38.

[Solution]

- Eq. 4.44: $I_B = \dfrac{V_{EE} - V_{BE}}{R_B + (\beta + 1) R_E}$;

$$I_B = \frac{20\,\text{V} - 0.7\,\text{V}}{240\,\text{k}\Omega + (90+1)240\,\text{k}\Omega} ;$$

$$I_B = \frac{19.3\,\text{V}}{422\,\text{k}\Omega} = 45.73\,\mu\text{A}$$

Example 4.6 Emitter-Follower Configuration Cont'd

and Eq. 4.45: $V_{CE_Q} = V_{EE} - I_E R_E = V_{EE} - (\beta + 1) I_B R_E$;

$$V_{CE_Q} = 20\,\text{V} - (90+1)(45.73\,\mu\text{A})(2\,\text{k}\Omega) = 20\,\text{V} - 8.32\,\text{V} \;;$$

$$\boxed{V_{CE_Q} = 11.68\,\text{V}}$$

- It follows that,

$$I_{E_Q} = (\beta + 1) I_B = (90+1)(45.73\,\mu\text{A}) \;; \qquad \boxed{I_{E_Q} = 4.16\,\text{mA}}$$

4.8 Common-Base Configuration

- Is unique in that the applied signal is connected to the emitter terminal and the base is at, or just above, ground potential.
- In the ac domain it has a very low input impedance, high output impedance, and good gain.

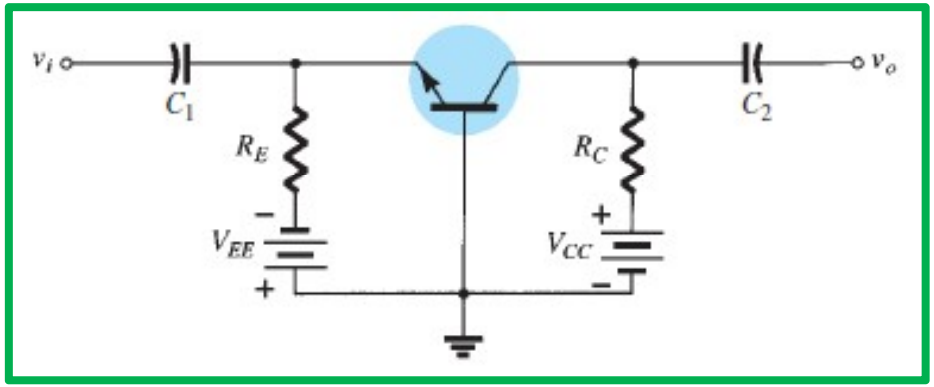


Figure 4.39: Common-base configuration.

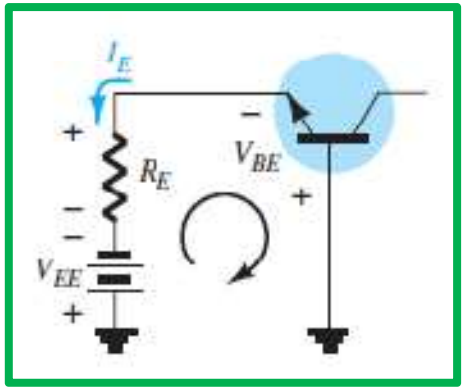


Figure 4.40: Input dc equivalent of Fig. 4.39.

- Applying Kirchhoff's voltage law to the input circuit yields

$$-V_{EE} + I_E R_E - V_{BE} = 0 \; ; \quad \Rightarrow \quad I_E = \frac{V_{EE} - V_{BE}}{R_E} \qquad [4.46]$$

4.8 Common-Base Configuration Cont'd

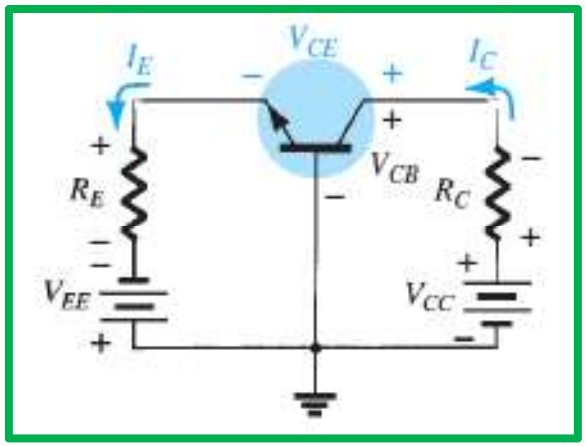


Figure 4.41: Determining V_{CE} and V_{CB} .

- Applying Kirchhoff's voltage law to the entire outside perimeter of the circuit of Fig. 4.41 yields

$$-V_{EE} + I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0 \; ;$$

$$\Rightarrow \; V_{CE} = V_{EE} + V_{CC} - I_E R_E - I_C R_C = 0 \; ;$$

- Let $I_E \cong I_C$ so that,

$$V_{CE} = V_{BE} + V_{CC} - I_E \left(R_C + R_E \right) \qquad [4.47]$$

- Applying KVL to the output loop of Fig. 4.41 gives

$$V_{CB} + I_C R_C - V_{CC} = 0 \; ; \quad \Rightarrow \; V_{CB} = V_{CC} - I_C R_C \; ;$$

- Let $I_E \cong I_C$ so that,

$$V_{CB} = V_{CC} - I_E R_C \qquad [4.48]$$

4.9 Multiple BJT Networks

- Thus far, the BJT circuits discussed have only been single-stage configurations.
- Let us briefly look at some of the most common multiple transistor networks.

RC Coupling

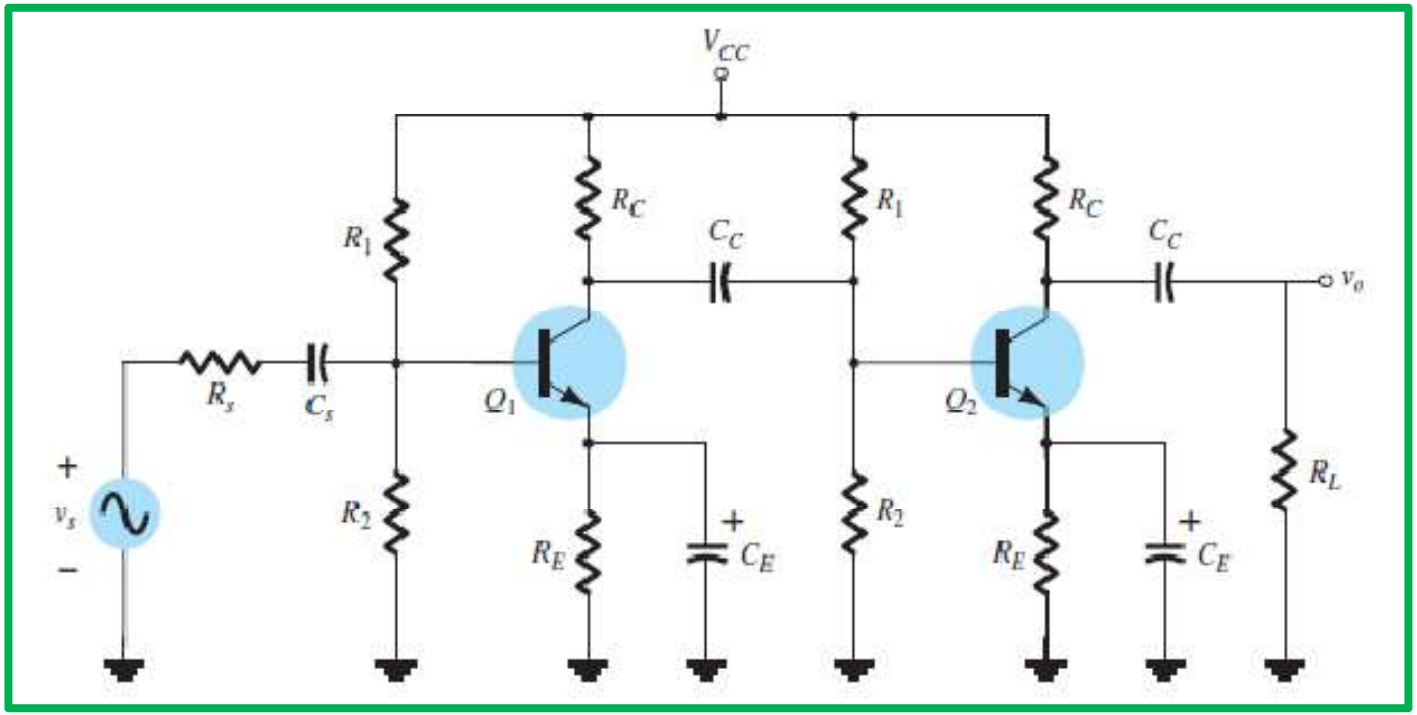


Figure 4.42: *RC* coupled BJT amplifiers.

4.9 Multiple BJT Networks Cont'd

- The network of Fig. 4.42 yields two dc bias circuits of Fig. 4.43 which can be analyzed as done before.

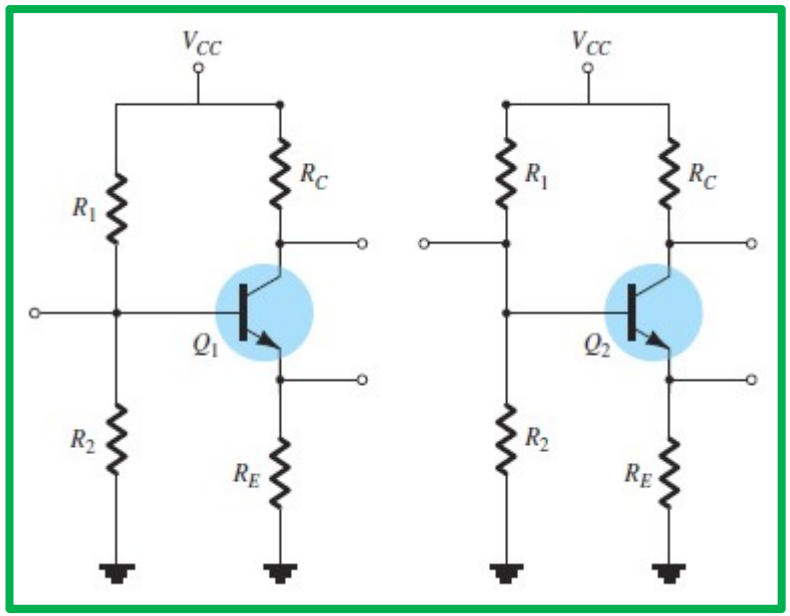


Figure 4.43: *DC* equivalent of Fig. 4.42.

Darlington Configuration

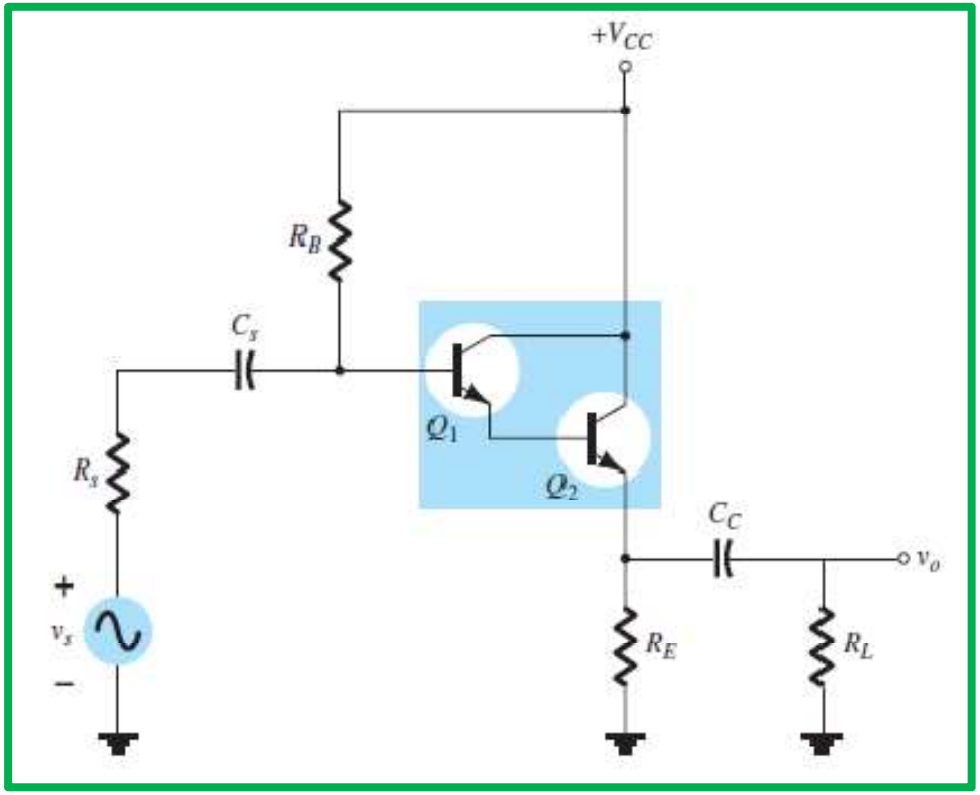


Figure 4.44: Darlington amplifier.

4.9 Multiple BJT Networks Cont'd

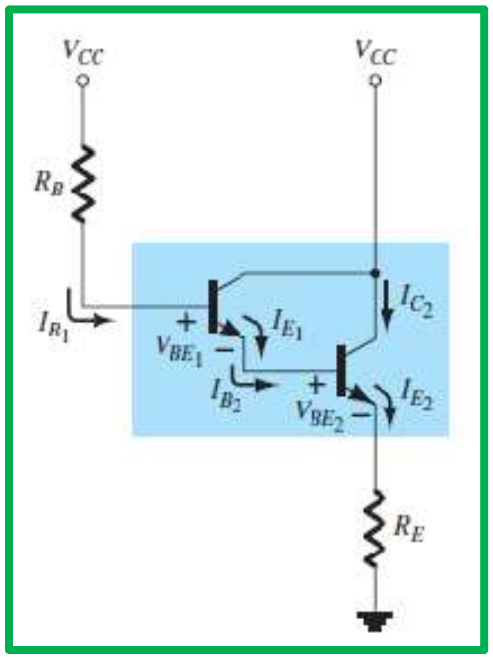


Figure 4.45: *DC* equivalent of Fig. 4.44.

- The Darlington amplifier of Fig. 4.44 feeds the output of one stage directly into the input of the succeeding stage.
- The input impedance is very high, making it attractive for use in amplifiers driven by sources of relatively high internal resistance.
- Assuming a beta β_1 for the first BJT and β_2 for the second BJT, it follows that

$$I_{B_2} = I_{E_1} = (\beta_1 + 1) I_{B_1}$$

- Furthermore,

$$I_{E_2} = (\beta_2 + 1) I_{B_2} = (\beta_2 + 1)(\beta_1 + 1) I_{B_1}$$

- Let $\beta \gg 1$ for each BJT, so that net beta for the configuration is

$$\beta_D = \beta_1 \beta_2 \qquad [4.49]$$

- This compares directly with a single-stage amplifier having a gain of β_D.

4.9 Multiple BJT Networks Cont'd

- Applying an analysis similar to that of section 4.4 yields

$$I_{B_1} = \frac{V_{CC} - V_{BE_1} - V_{BE_2}}{R_B + (\beta_D + 1)R_E}$$

- Defining

$$V_{BE_D} = V_{BE_1} + V_{BE_2} \qquad [4.50]$$

- We have.

$$I_{B_1} = \frac{V_{CC} - V_{BE_D}}{R_B + (\beta_D + 1)R_E} \qquad [4.51]$$

- The currents

$$I_{C_2} \cong I_{E_2} = \beta_D I_{B_1} \qquad [4.52]$$

- The dc voltage at the emitter terminal is

$$V_{E_2} = I_{E_2} R_E \qquad [4.53]$$

- Vividly,

$$V_{C_2} = V_{CC} \qquad [4.54]$$

4.9 Multiple BJT Networks Cont'd

- Thus, the voltage across the output of transistor is

$$V_{CE_2} = V_{C_2} - V_{E_2} \quad ; \quad \boxed{V_{BE_D} = V_{BE_1} + V_{BE_2}} \qquad [4.55]$$

- There are many other multiple transistor networks which will not be discussed in lecture 4. Nevertheless, you ought to take keen interest, in your spare time, to look at and understand.
- These include:

Cascode Configuration

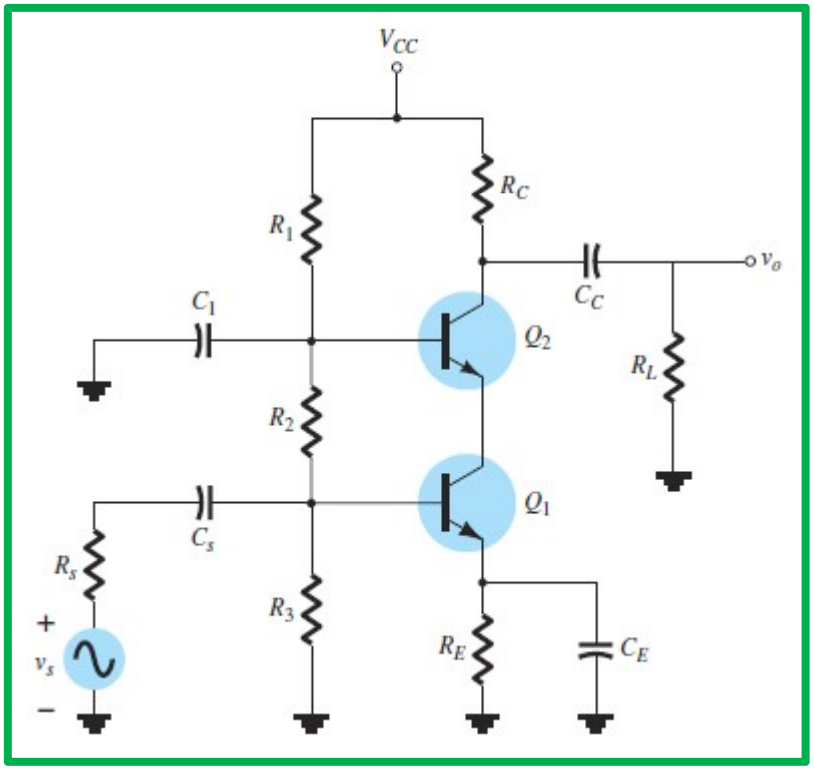


Figure 4.46: Cascode Amplifier.

4.9 Multiple BJT Networks Cont'd

Feedback Pair Amplifier

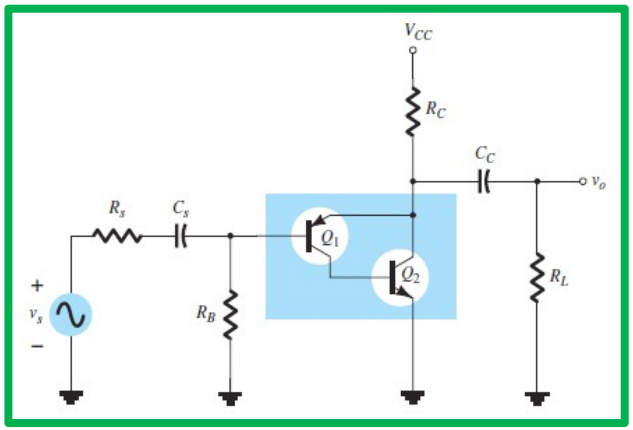


Figure 4.47: Feedback Amplifier.

Direct Coupled Amplifier

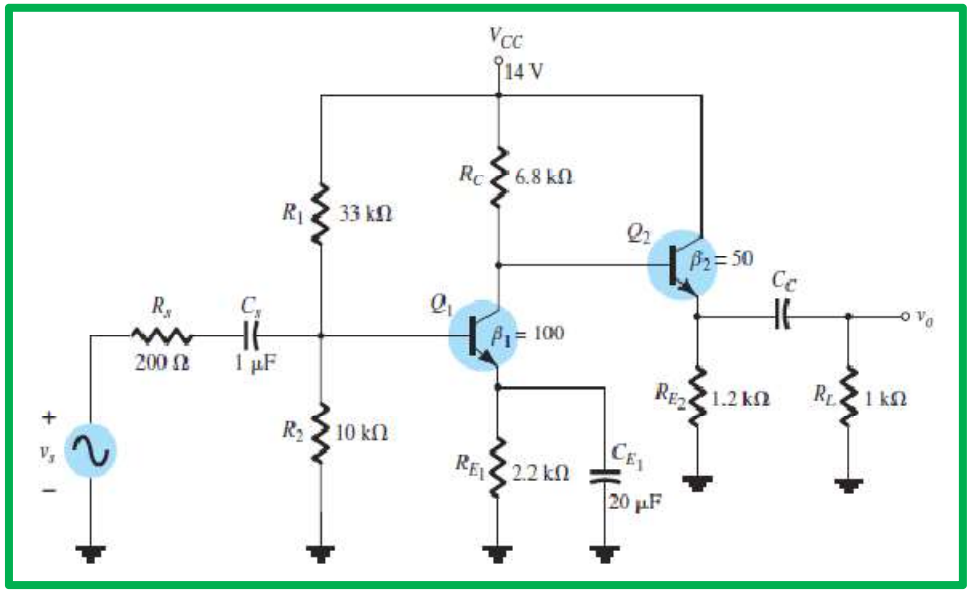


Figure 4.48: Direct-coupled Amplifier.

Current Mirror

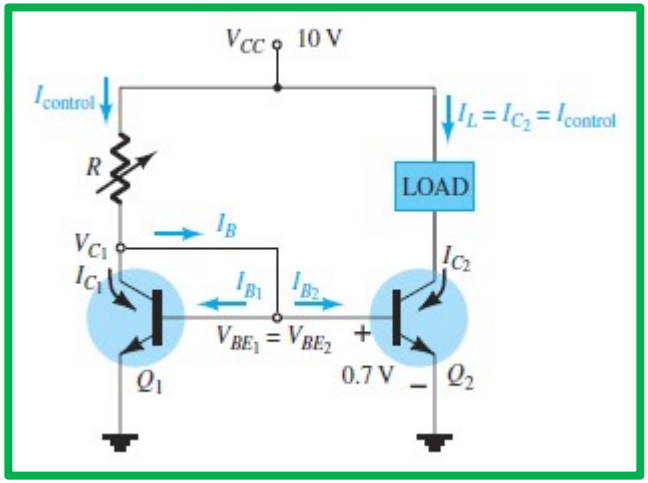


Figure 4.49: Current mirror using back-to-back BJTs.

4.10 *pnp* BJTs

- Thus far, the analysis has been based on *npn* transistors.
- It is worth noting that the analysis of *pnp* transistors follows the same pattern, except that the resulting equations have change of signs associate with particular quantities.
- For instance, notice the change of signs in Fig. 4.50.

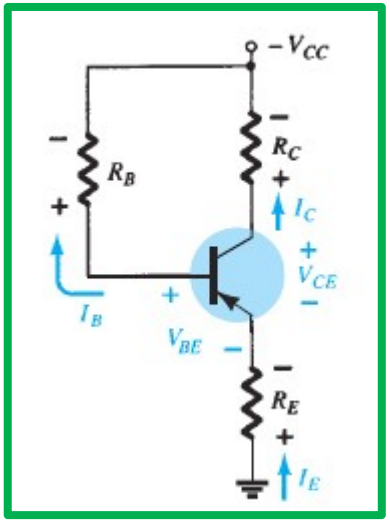
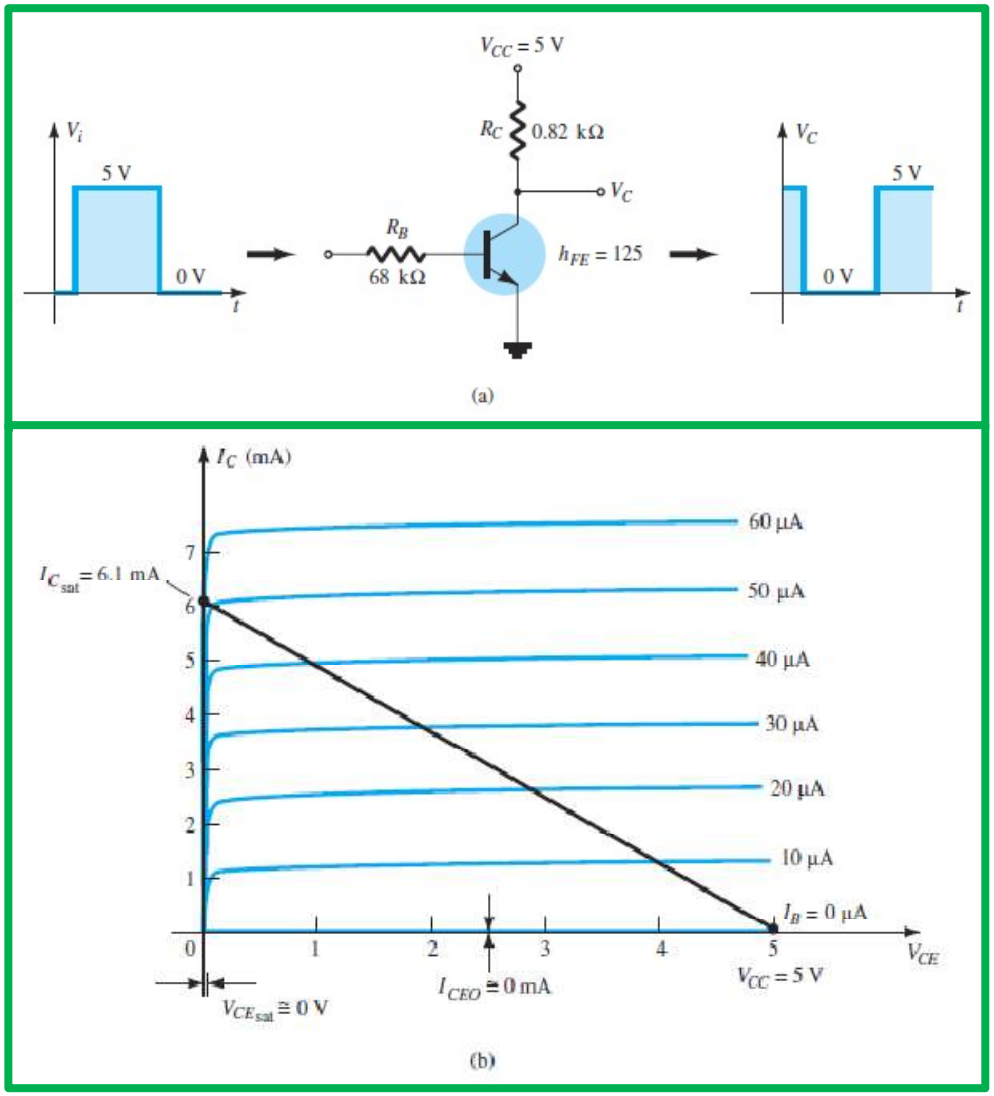


Figure 4.50: pnp BJT in an emitter stabilized configuration

4.11 Transistor Switching Networks

- Transistor applications are not limited solely to the amplification of signals.
- Through proper design, BJTs can be used as switches for computer logic circuits and control applications.

4.11 Transistor Switching Networks Cont'd



- Proper design for the inversion process requires that the operating point switch from cutoff to saturation along the load line depicted in Fig. 4.51.
- For this purpose assume $I_C = I_{CEO} \cong 0\,\text{mA}$ when $I_B = 0\,\mu\text{A}$ and $V_{CE} = V_{CE_{sat}} \cong 0\,\text{V}$.
- When $V_i = 5\,\text{V}$, the BJT will be "ON" and the design must ensure that the network is heavily saturated by a level of $I_B > 50\,\mu\text{A}$.

Figure 4.51: Transistor inverter

4.11 Transistor Switching Networks Cont'd

- The saturation level for the collector current is

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C} \qquad [4.56]$$

- The level of I_B in the active region just before saturation results can be approximated by

$$I_{B_{\max}} \cong \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}}$$

- For the saturation level we must therefore ensure that the following condition is met:

$$I_B > \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}} \qquad [4.57]$$

- For the network of Fig. 4.51, when $V_i = 5\,\text{V}$, then

$$I_B = \frac{V_i - 0.7\,\text{V}}{R_B} = \frac{5\,\text{V} - 0.7\,\text{V}}{68\,\text{k}\Omega} = 63\,\mu\text{A}$$

4.11 Transistor Switching Networks Cont'd

- Furthermore

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C} = \frac{5\,\text{V}}{0.82\,\text{k}\Omega} \cong 6.1\,\text{mA}$$

- Testing Eq. [4.57] yields

$$I_B = 63\,\mu\text{A} > \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}} = \frac{6.1\,\text{mA}}{125} = 48.8\,\mu\text{A}$$

- For $V_i = 0\,\text{V}$, $I_B = 0\,\mu\text{A}$, and assuming that $I_C = I_{CEO} = 0\,\text{mA}$, the voltage drop across R_C as determined by $V_{R_C} = I_C R_C = 0\,\text{V}$, resulting in $V_C = +5\,\text{V}$ for the response indicated in Fig. 4.51a.

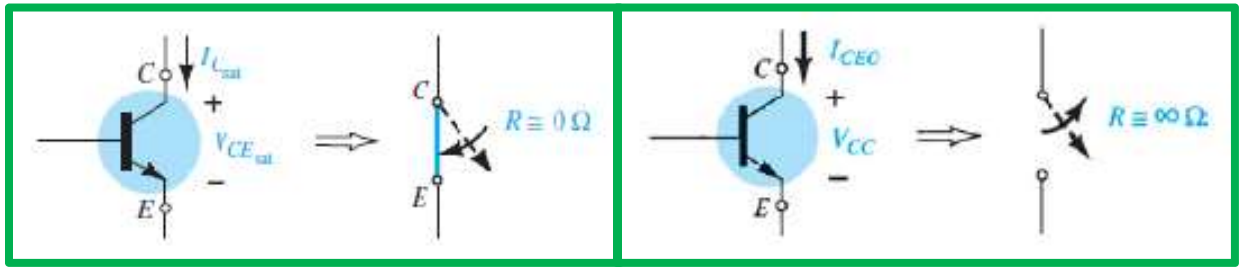


Figure 4.52: Saturation conditions and resulting resistance.

Figure 4.53: Cutoff conditions and resulting resistance.

$$R_{\text{sat}} = \frac{V_{CE_{\text{sat}}}}{I_{C_{\text{sat}}}}$$

$$R_{\text{cutoff}} = \frac{V_{CC}}{I_{CEO}}$$

4.12 Bias Stabilization

- Stability of a system is a measure of the sensitivity of a network to variations in its parameters.

- β : increases with increase in temperature
- $|V_{BE}|$: decreases about $2.5\,\text{mV}$ per degree Celsius $(^{\circ}C)$ increase in temperature
- I_{CO} (reverse saturation current): doubles in value for every 10°C increase in temperature.

Stability Factors

- Defined for each parameter affecting bias as follows:

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}} \qquad [4.58]$$

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}} \qquad [4.59]$$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} \qquad [4.60]$$

4.12 Bias Stabilization Cont'd

S(I_{CO})

- **Fixed-Bias Configuration**

$$S(I_{CO}) \cong \beta \qquad [4.61]$$

- **Emitter-Bias Configuration**

$$S(I_{CO}) \cong \frac{\beta(1 + R_B/R_E)}{\beta + R_B/R_E} \qquad [4.62]$$

- **Voltage-Divider Bias Configuration**

$$S(I_{CO}) \cong \frac{\beta(1 + R_{Th}/R_E)}{\beta + R_{Th}/R_E} \qquad [4.63]$$

- **Feedback-Bias Configuration (R_E = 0 Ω)**

$$S(I_{CO}) \cong \frac{\beta(1 + R_B/R_C)}{\beta + R_B/R_C} \qquad [4.64]$$

4.12 Bias Stabilization Cont'd

S(V_{BE})

- **Fixed-Bias Configuration**

$$S(V_{BE}) \cong -\beta / R_B \qquad [4.65]$$

- **Emitter-Bias Configuration**

$$S(V_{BE}) \cong \frac{-\beta / R_E}{\beta + R_B / R_E} \qquad [4.66]$$

- **Voltage-Divider Bias Configuration**

$$S(V_{BE}) \cong \frac{-\beta / R_E}{\beta + R_{\mathrm{Th}} / R_E} \qquad [4.67]$$

- **Feedback-Bias Configuration (R_E = 0 Ω)**

$$S(I_{CO}) \cong \frac{-\beta / R_C}{\beta + R_B / R_C} \qquad [4.68]$$

4.12 Bias Stabilization Cont'd

S(β)

- **Fixed-Bias Configuration**

$$S(\beta) \cong I_{C_1} / \beta_1 \qquad [4.69]$$

- **Emitter-Bias Configuration**

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C_1}\left(1 + R_B / R_E\right)}{\beta_1\left(\beta_2 + R_B / R_E\right)} \qquad [4.70]$$

- **Voltage-Divider Bias Configuration**

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C_1}\left(1 + R_{\mathrm{Th}} / R_E\right)}{\beta_1\left(\beta_2 + R_{\mathrm{Th}} / R_E\right)} \qquad [4.71]$$

- **Feedback-Bias Configuration (R_E = 0 Ω)**

$$S(\beta) = \frac{I_{C_1}\left(R_B + R_C\right)}{\beta_1\left(R_B + \beta_2 R_C\right)} \qquad [4.72]$$

End of Lecture 4

Thank you for your attention!