EEE 3571 Electronic Engineering I

Lecture 5: Bipolar Junction Transistor AC Analysis

May 2022

Dr. Daliso Banda

daliso.banda@unza.zm

Department of Electrical & Electronic Engineering, School of Engineering, University of Zambia

References

Our main reference text books in this course are

[1] Neil S., Electronics: A Systems Approach, 4th edition, 2009, Pearson Education Limited, ISBN 978-0-273-71918-2.

[2] Boylestad R. L., Nashelsky L., Electronic Devices and Circuit Theory, 11th Ed, 2013, Prentice-Hall, ISBN 978-0-13-262226-4.

[3] Smith R. J., Dorf R. C., Circuits Devices and Systems, 5th Ed., 2004, John Wiley, ISBN ISBN 9971-51-172-X.

However, feel free to use pretty much any additional text which you might find relevant to our course.

Learning Objectives

At the end of the lecture 5 on BJT AC Analysis, you ought to:

1) Become familiar with the r_e, hybrid, and hybrid π models for the BJT transistor.
2) Learn to use the equivalent model to find the important ac parameters for an amplifier.
3) Understand the effects of a source resistance and load resistor on the overall gain and characteristics of an amplifier.
4) Become aware of the general ac characteristics of a variety of important BJT configurations.
5) Begin to understand the advantages associated with the two-port systems approach to single- and multistage amplifiers.
6) Develop some skill in troubleshooting ac amplifier networks.

5.1 Introduction

- The basic construction, appearance, and characteristics of the BJT were introduced in lecture 3. The dc biasing of the device was then examined in detail in lecture 4.
- Now we begin to examine the ac response of the BJT amplifier based on models most frequently used.
- The first concern in the sinusoidal ac analysis of transistor networks is the magnitude of the input signal.
- It will determine whether small-signal or large-signal techniques should be employed.
- The small-signal technique is introduced in this lecture and the large-signal applications will be examined in future lectures.
- Common models used in small-signal ac analysis of the transistor are: r_e hybrid model, hybrid π model, and the hybrid equivalent model.

5.2 Amplification in the AC Domain

- Amplification means the output sinusoidal signal is greater than the input sinusoidal signal.
- Stated another way, the output ac power is greater than the input ac power.
- However, the law of conservation of energy dictates that over time the total power output, P_o, of a system cannot be greater than its input, P_i.
- Thus, the efficiency $\eta = P_o / P_i$ cannot be greater than 1.
- Nevertheless, in transistor amplifiers the factor that permits an ac power output greater than the input ac power is the applied dc power.
- Thus, conversion efficiency is defined by $\eta = P_{o(\text{ac})} / P_{i(\text{dc})}$, where $P_{o(\text{ac})}$ is the ac power to the load and $P_{i(\text{dc})}$ is the dc power supplied.

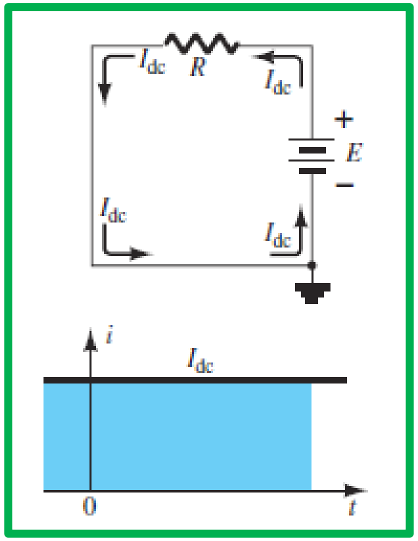


Figure 5.1: Steady current established by a dc supply.

5.2 Amplification in the AC Domain Cont'd

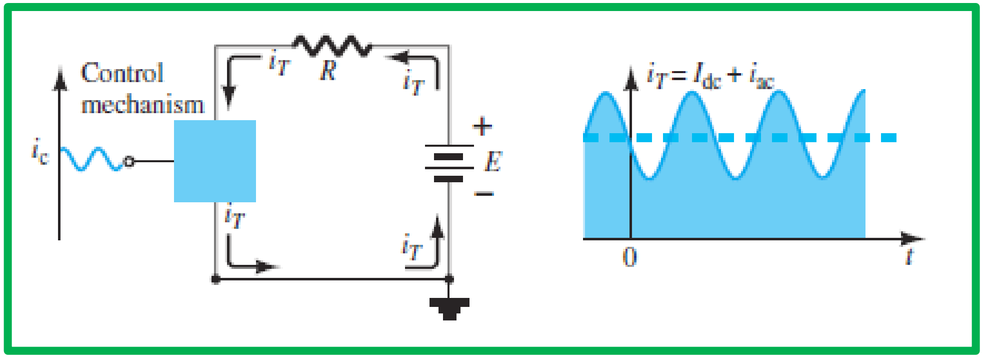


Figure 5.2: Effect of a control element on the steady-state flow of the electrical system of Fig. 5.1.

- Let us now insert a control mechanism such as that shown in Fig. 5.2.
- The control is such that the application of a relatively small signal to control mechanism results in substantial oscillation in the output circuit.
- That is, for example $i_{ac(p\text{-}p)} \gg i_{c(p\text{-}p)}$
- For the system of Fig. 5.2, the peak value of the oscillation in the output circuit is controlled by the established dc level.
- Any attempt to exceed the limit set by the dc level will result in a "clipping" (flattening) of the negative and positive peaks.
- In general, proper amplification design entails that the dc and ac components be sensitive to each other's requirements and limitations.

5.3 BJT Transistor Modeling

- The key in small-signal analysis is the use of the equivalent circuits (models).
- A model is a combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions.
- In the formative years of BJT analysis the *hybrid equivalent network* was use most often.
- In time the use of the r_e *model* became the more desirable approach since vital parameters of the equivalent circuit were determined by the actual operating conditions as opposed to use of data sheets.
- Nevertheless, the designer ought to still use the data sheets for some other parameters of the equivalent circuit.
- Furthermore, the r_e *model* failed to include a feedback term which is vital in some cases.

5.3 BJT Transistor Modeling Cont'd

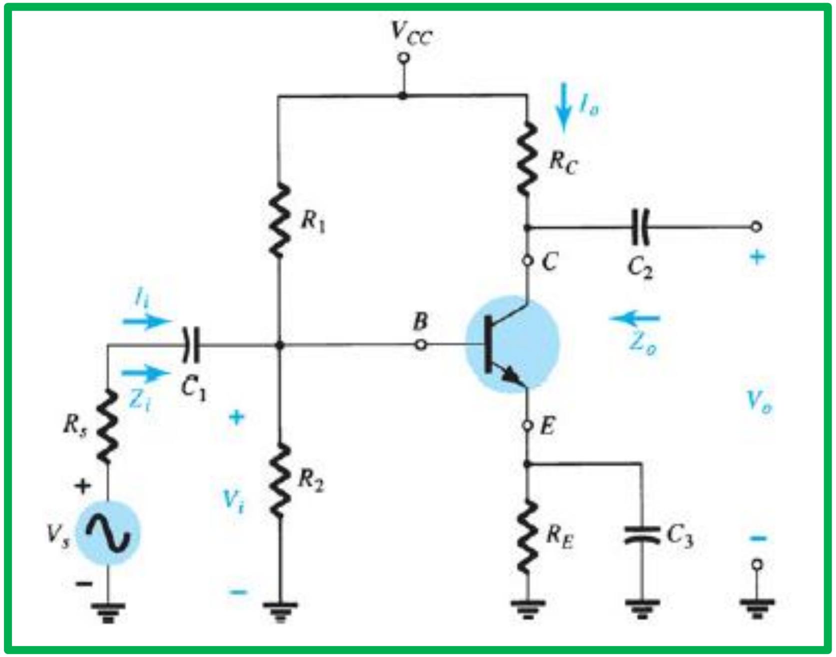


Figure 5.3: BJT circuit under examination.

- Capacitors chosen to have very small reactance at signal frequency.
- Network of Fig. 5.3 with dc supply removed and capacitors short-circuited depicted in Fig. 5.4.

- To demonstrate the impact of the ac equivalent circuit on analysis to follow, consider Fig. 5.3.
- Since we need to determine the ac response, replace all the dc voltage sources with short circuits, as they only set the dc (quiescent level) of the output voltage.

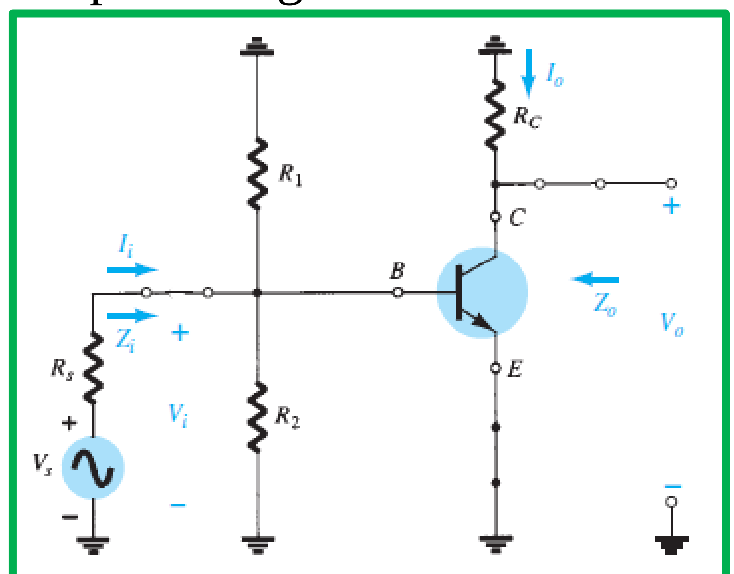


Figure 5.4

5.3 BJT Transistor Modeling Cont'd

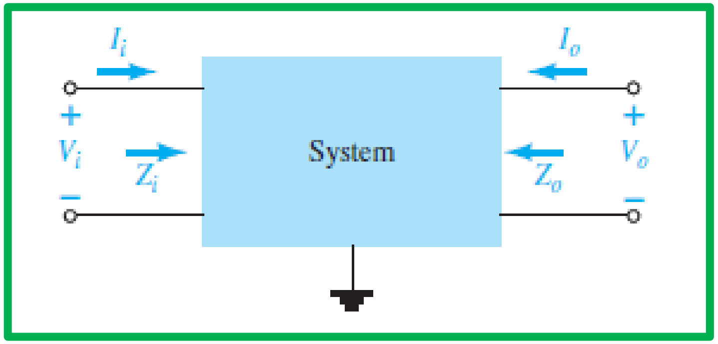


Figure 5.5: Defining vital parameters of any system.

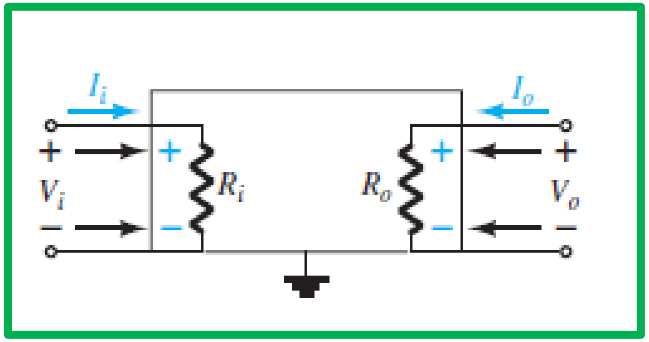


Figure 5.6: Demonstrating the reason for the define directions and polarities.

- We define vital parameters being:
- Input impedance $Z_i = V_i / I_i$ obtained "looking into" the system.
- Output impedance $Z_o = V_o / I_o$ determined "looking back into" the system.
- Thus, keep Fig. 5.5 in mind as you analyze the BJT networks in lecture 5.
- It is a vital introduction to "System Analysis" which is becoming important with the expanded use of packaged Integrated Circuit (IC) systems.

5.3 BJT Transistor Modeling Cont'd

- If we establish a common ground and rearrange the elements of Fig. 5.4 $R_1 \| R_2$ as shown in Fig. 5.7.
- Analysis tools such as superposition, Thevenin's theorem, and so forth, can be exploited to determine the quantities sought.
- Since the BJT is an amplifying device, ought to determine the voltage gain

$$A_v = V_o / V_i$$

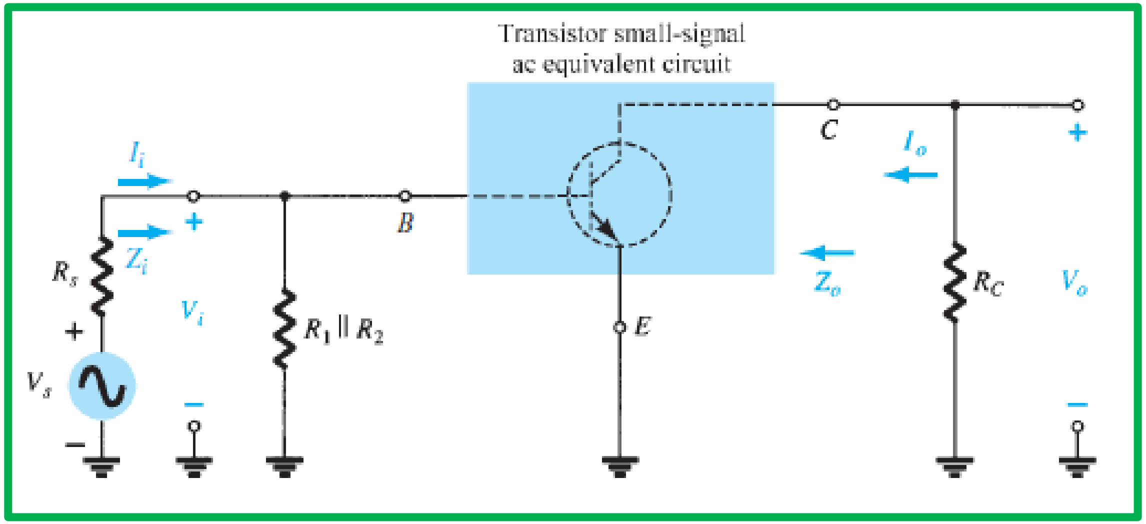


Figure 5.7: Circuit of Fig. 5.4 redrawn for small-signal ac analysis.

- Note in Fig. 5.7 that the current gain is defined as

$$A_i = I_o / I_i$$

- The sections to follow will introduce a transistor equivalent model to complete ac analysis of Fig. 5.7.

5.4 The r_e Transistor Model

- The r_e *model* for the CE, CB, and CC BJT transistor configurations will now be introduced.

Common-Emitter Configuration

- Equivalent circuit for CE is constructed using the device characteristics and a number of approximations.
- Looking at the input side, it turns out the applied voltage V_i is equal to the voltage V_{be} with input current being the base current I_b, see Fig. 5.8.
- Recall from lecture 3 that the current through the forward-biased junction of the BJT is I_E, thus the characteristics for the input side are as shown in Fig. 5.9a subject to various levels of V_{BE}.

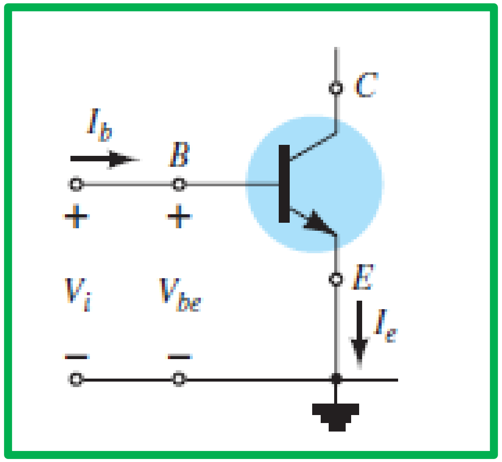


Figure 5.8: Finding the input equivalent circuit for a BJT.

5.4 The r_e Transistor Model Cont'd

- Taking the average values of the curves in Fig. 5.9a will result in the single curve of Fig. 5.9b, which is simply a forward-biased diode.

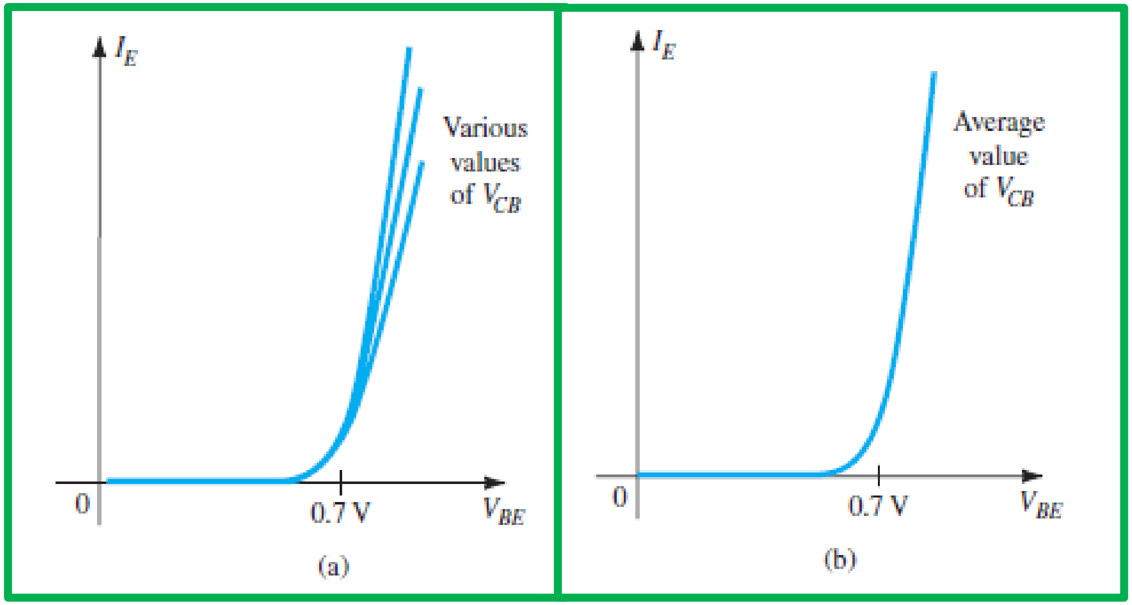


Figure 5.9: Defining the average curve for the characteristics of Fig. 5.9a.

- Thus, Fig. 5.10 depicts a single diode equivalent circuit with a current I_e .
- We now ought to add a component to the network that will establish the current I_e of Fig. 5.10 using the characteristics.

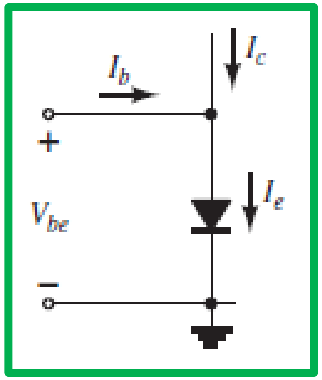


Figure 5.10: Equivalent circuit for the input side of BJT.

5.4 The r_e Transistor Model Cont'd

- Redrawing the collector characteristics approximately to have a constant β as shown in Fig. 5.11, we can thus replace the entire characteristics at the output section by a controlled source whose magnitude is beta times the base current.

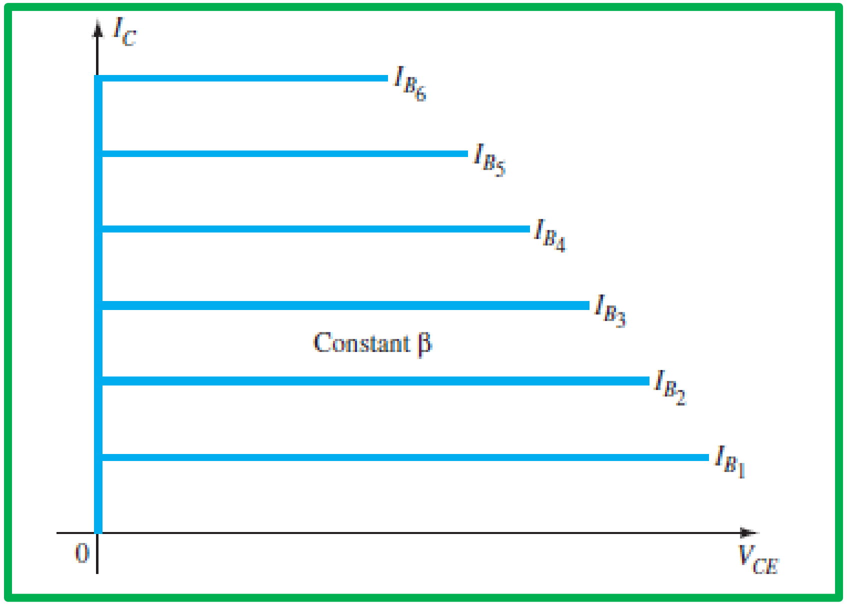


Figure 5.11: Constant β characteristics.

- Thus, the equivalent network for the common-emitter configuration has been established in Fig. 5.12.
- This model is awkward to work with due to the direct connection between output and input.

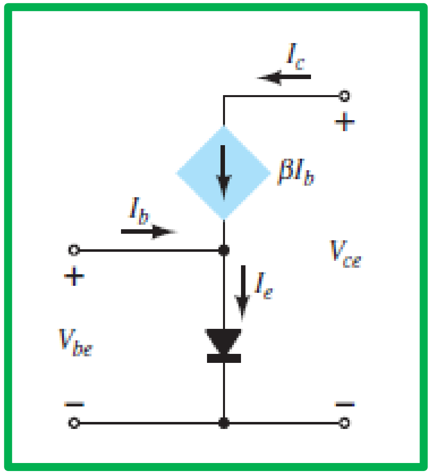


Figure 5.12: BJT equivalent circuit.

5.4 The r_e Transistor Model Cont'd

- Thus, the Fig. 5.12 is improved by replacing the diode with its equivalent resistance, see Fig. 5.13.

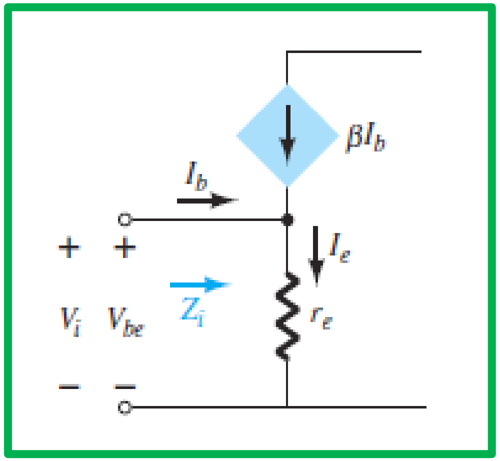


Figure 5.13: Defining the level of Z_i.

- Recall that the diode resistance is determined by $r_D = 26\,\mathrm{mV}/I_D$.
- We resort the use of subscript *e* since the determining current is I_E , this yields $r_e = 26\,\mathrm{mV}/I_E$.
- Now for the input side: $Z_i = \dfrac{V_i}{I_b} = \dfrac{V_{be}}{I_b}$
- Solving for V_{BE} yields,

$$V_{be} = I_e r_e = (I_c + I_b) r_e = (\beta I_b + I_b) r_e \;;\quad \Rightarrow V_{be} = (\beta + 1) I_b r_e$$

- It follows that,

$$Z_i = \frac{V_{be}}{I_b} = \frac{(\beta+1) I_b r_e}{I_b} \;; \Rightarrow \quad \boxed{Z_i = (\beta+1) r_e \cong \beta r_e} \qquad [5.1]$$

5.4 The r_e Transistor Model Cont'd

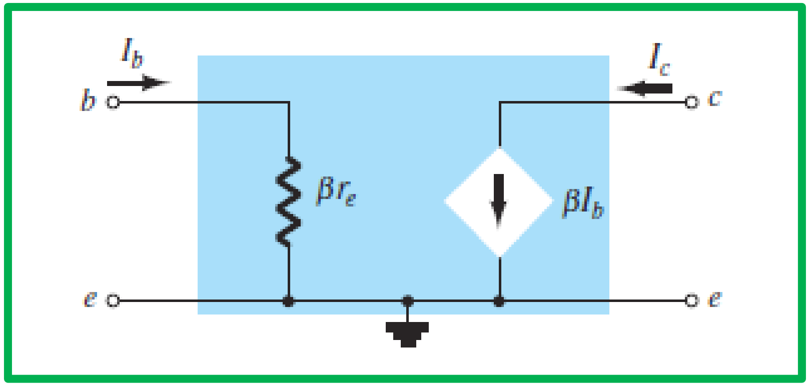


Figure 5.14: Improved BJT equivalent circuit.

- The equivalent circuit for the ideal characteristics of Fig. 5.11 with input and output circuits isolated is shown in Fig. 5.14.
- Notice that input and output circuits are still linked via the dependent (controlled) current source.

Early Voltage

- In reality the characteristics are not ideal as depicted in Fig. 5.11, but as shown in Fig. 5.15.

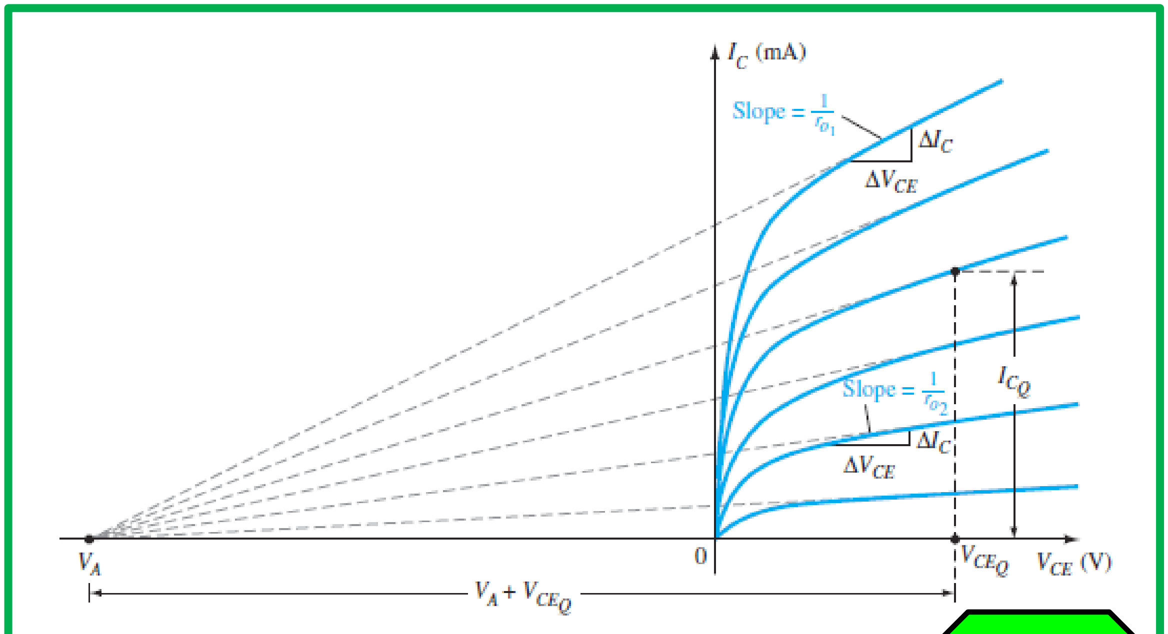


Figure 5.15: Defining the Early voltage and output impedance of a BJT.

5.4 The r_e Transistor Model Cont'd

- Note that slope of the characteristics defines the output impedance.
- Thus, the steeper the slope, the less the output impedance and the less ideal the BJT.
- Generally, large output impedance is desirable to avoid loading down the next stage of a design.
- For a particular collector and base current as shown in Fig. 5.15, the output impedance is determined using the equation

$$\boxed{r_o = \frac{\Delta V}{\Delta I} = \frac{V_A + V_{CE_Q}}{I_{C_Q}}} \qquad [5.2]$$

- Typically, the Early voltage $V_A \gg V_{CE_Q}$ to permit the approximation;

$$\boxed{r_o \cong \frac{V_A}{I_{C_Q}}} \qquad [5.3]$$

- Vividly V_A is fixed, thus as $I_{C_Q} \uparrow$, $r_o \downarrow$.

5.4 The r_e Transistor Model Cont'd

- For situations where V_A is unknown the output impedance r_o can be found from the characteristics at any base or collector current using the equation;

$$\text{slope} = \frac{\Delta y}{\Delta x} = \frac{\Delta I_C}{\Delta V_{CE}} = \frac{1}{r_o}\,; \quad \Rightarrow \quad \boxed{r_o = \frac{\Delta V_{CE}}{\Delta I_C}} \qquad [5.4]$$

- Including the output impedance in the equivalent circuit of Fig. 5.15 completes the r_e model depicted in Fig. 5.16.

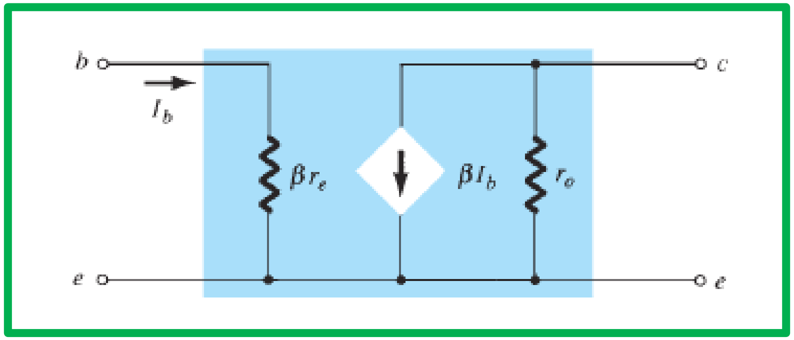


Figure 5.16: r_e model for the common-emitter BJT configuration including effects of r_o .

- Thus, the r_e model of Fig. 5.16 will now be used through the analysis to follow for common-emitter configuration.

5.4 The r_e Transistor Model Cont'd

Common-Base Configuration

- Its equivalent circuit is developed in much the same manner as was the case for common-emitter configurations.

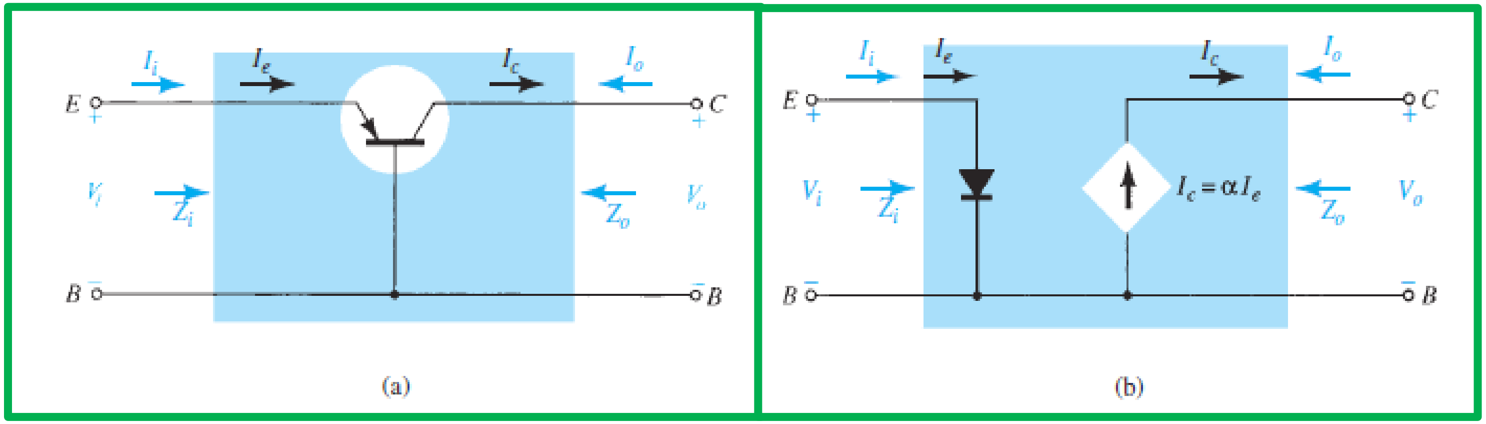


Figure 5.17: (a) Common-base BJT; (b) equivalent circuit for CB configuration.

- Notice that since the *pnp* BJT is employed in Fig. 5.16a, the controlled (depended) source defining the collector current is opposite in direction to that of npn BJT CE configuration discussed earlier.
- Thus, the collector current in the output circuit is now opposite that of the defined output current.

5.4 The r_e Transistor Model Cont'd

- For the ac response, the diode in Fig. 5.17 can be replaced by its ac resistance given by $r_e = 26\text{mA}/I_E$ as shown in Fig. 5.18.

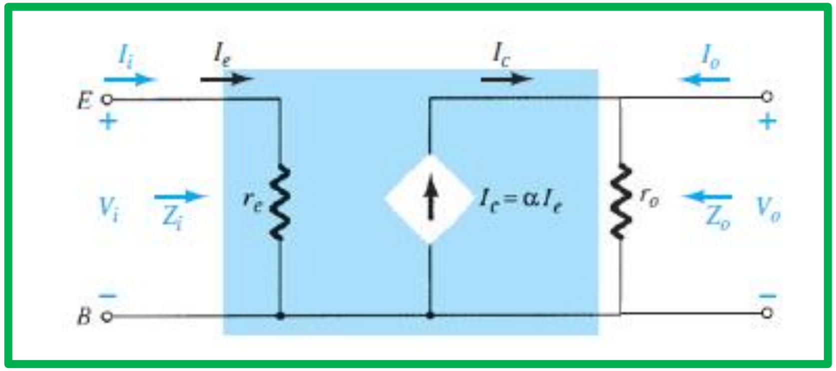


Figure 5.18: Common-base r_e equivalent circuit.

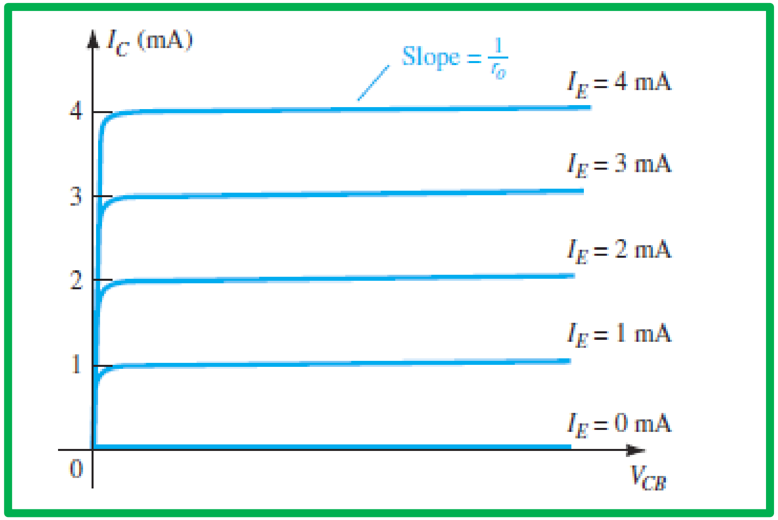


Figure 5.19: Defining Z_o.

- In general, CB configurations have low input impedance since it is essentially simply r_e with typical values ranging from a few ohms to perhaps 50 Ω.
- The output impedance r_o will typically extend into the mega ohm range.
- Note that there is no phase shift between the input and output voltages for CB, as opposed to CE which has 180° phase shift.

5.4 The r_e Transistor Model Cont'd

Common-Collector Configuration

- For the common-collector configuration, the model defined for CE of Fig. 5.16 is normally applied rather than defining a model for CC configuration.

npn versus *pnp*

- The dc analysis of npn and pnp configurations is quite different in the sense that currents will have opposite directions and voltages opposite polarities.
- However, for an ac analysis where the signal will progress between positive and negative, the ac equivalent circuit will be the same.

5.5 Common-Emitter Fixed-Bias Configuration

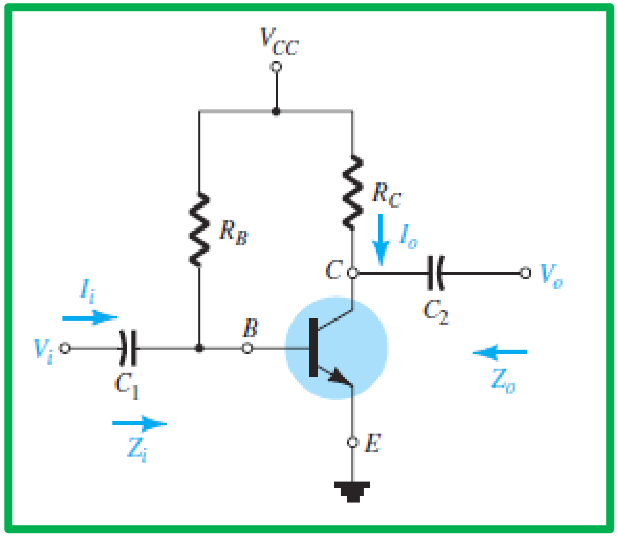


Figure 5.20: Common-emitter fixe-bias configuration.

- ❑ The BJT models just introduced will now be used to perform a small-signal ac analysis.

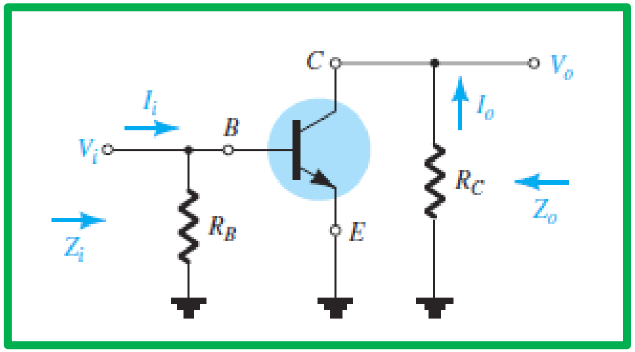


Figure 5.21: Network of Fig. 5.20 after removal of V_{CC}, C_1 and C_2.

- ❑ The next step is to determine β, r_e , and r_o.
- ❑ The magnitude of β is typically obtained from a specification sheet or by measurement with a curve tracer.

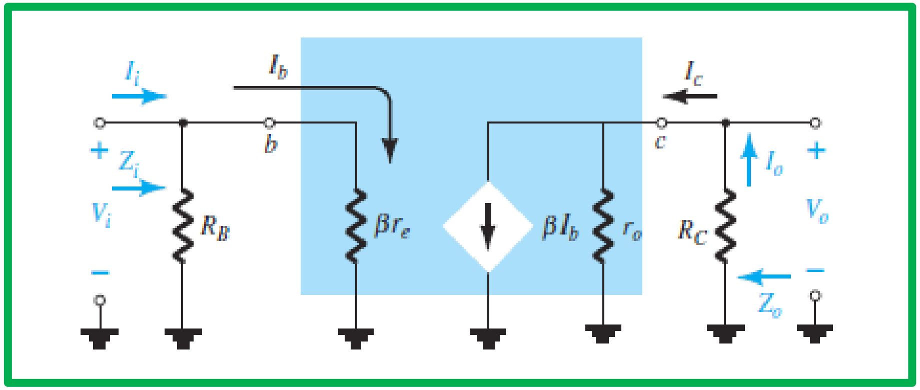


Figure 5.22: Substituting the r_e model into Fig. 5.21.

5.5 Common-Emitter Fixed-Bias Configuration Cont'd

- The value of r_e must be determined from dc analysis of the system.
- The magnitude of r_o.is typically obtained from the specification sheet or characteristics.
- Once β, r_e , and r_o are known, the following equations are realised from the two-port characteristics of the system.
- ***Z_i*** Fig. 5.22 clearly shows that

$$\boxed{Z_i = R_B \| \beta r_e \quad [\Omega]} \tag{5.5}$$

- The following approximation can be made subject the condition indicated

$$\boxed{Z_i \cong \beta r_e \Big|_{R_B \geq 10\beta r_e} \quad [\Omega]} \tag{5.6}$$

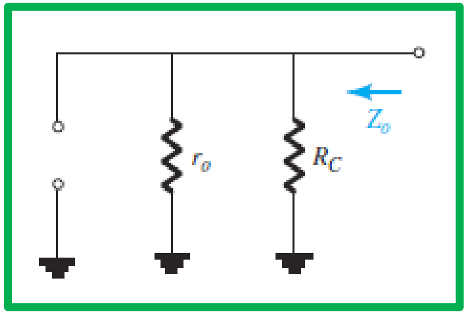


Figure 5.23: Determining Z_o for the circuit of Fig. 5.22.

- ***Z_o*** Recall that the output impedance of any system is defined as the impedance Z_o determined when $V_i = 0$.
- For Fig. 5.22, when $V_i = 0$, $I_i = I_b = 0$, this yields

$$\boxed{Z_o = R_C \| r_o \quad [\Omega]} \tag{5.7}$$

5.5 Common-Emitter Fixed-Bias Configuration Cont'd

- The approximation is frequently used subject to meeting the constraint given

$$Z_o \cong R_C \Big|_{r_o \geq 10R_C} \ [\Omega] \tag{5.8}$$

- ***A_V*** The voltage gain is obtained as follows,

$$V_o = -\beta I_b \left(R_C \| r_o \right) ;$$

- But

$$I_b = \frac{V_i}{\beta r_e} ; \quad \Rightarrow V_o = -\beta \left(\frac{V_i}{\beta r_e} \right) \left(R_C \| r_o \right) ;$$

- Thus,

$$A_v = \frac{V_o}{V_i} = -\frac{\left(R_C \| r_o \right)}{r_e} \tag{5.9}$$

- If $r_o \geq 10R_C$, so that the effect of r_o can be ignored,

$$A_v \cong -\frac{R_C}{r_e} \Bigg|_{r_o \geq 10R_C} \tag{5.10}$$

5.5 Common-Emitter Fixed-Bias Configuration Cont'd

Phase Relationship

- The negative sign in the resulting equation for A reveals that a 180° phase shift occurs between the input and output signals, as shown in Fig. 5.24.

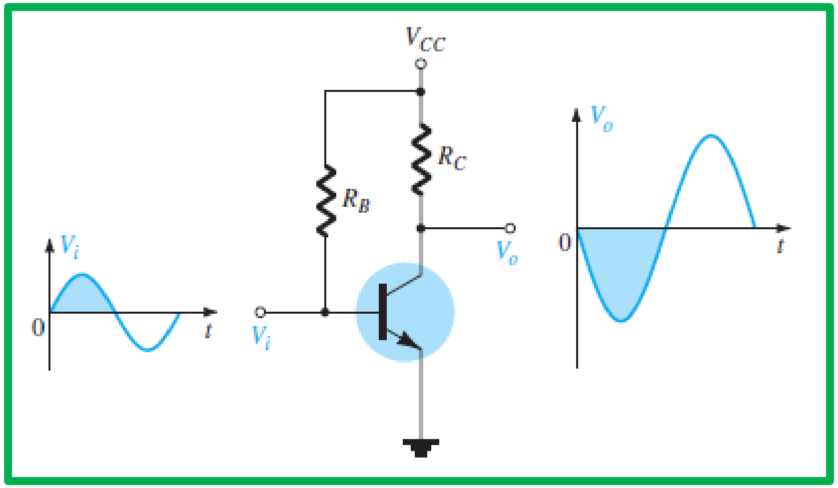
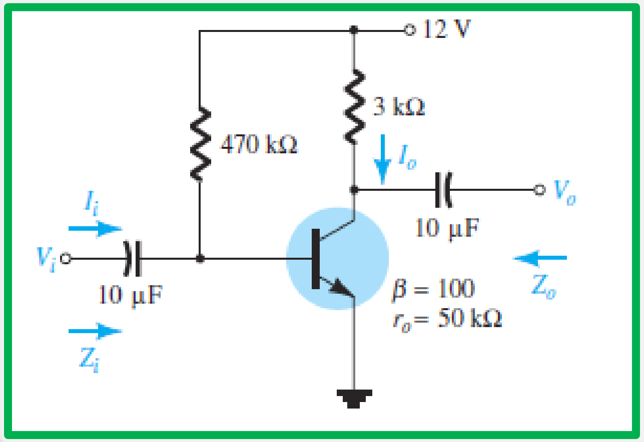


Figure 5.24: Demonstrating the 180° phase shift between input and output waveforms.

Example 5.1 Fixed-Bias Configuration



- For the network of Fig. 5.25:

a) Determine r_e.

b) Find Z_i (with $r_o = \infty\Omega$) .

c) Calculate Z_o (with $r_o = \infty\Omega$) .

d) Determine A_v (with $r_o = \infty\Omega$).

Figure 5.25: Example 5.1.

Example 5.1 Fixed-Bias Configuration Cont’d

e) Repeat parts (c) and (d) including $r_o = 50\,\text{k}\Omega$ in all the calculations and compare the results.

[Solution]

a) DC Analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\,\text{V} - 0.7\,\text{V}}{470\,\text{k}\Omega} = 24.04\,\mu\text{A}$$

$$I_E = (\beta + 1) I_B = (101)(24.04\,\mu\text{A}) = 2.428\,\text{mA}$$

$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{2.428\,\text{mA}} = \mathbf{10.71\,\Omega}$$

b) $\beta r_e = (100)(10.71\Omega) = 1.071\,\text{k}\Omega$

$$Z_i = R_B \| \beta r_e = 470\,\text{k}\Omega \| 1.071\,\text{k}\Omega = \mathbf{1.07\,k\Omega}$$

c) $Z_o = R_C = \mathbf{3\,k\Omega}$

d) $A_v = -\frac{R_C}{r_e} = -\frac{3\,\text{k}\Omega}{10.71\,\Omega} = \mathbf{-280.11}$

Example 5.1 Fixed-Bias Configuration Cont'd

e) $Z_o = r_o \| R_C = 50\,\text{k}\Omega \| 3\,\text{k}\Omega = \mathbf{2.83\,k\Omega}$ vs $3\,\text{k}\Omega$

$$A_v = -\frac{r_o \| R_C}{r_e} = -\frac{2.83\,\text{k}\Omega}{10.71\,\text{k}\Omega} = \mathbf{-264.24} \text{ vs } -280.11$$

5.6 Voltage-Divider Bias

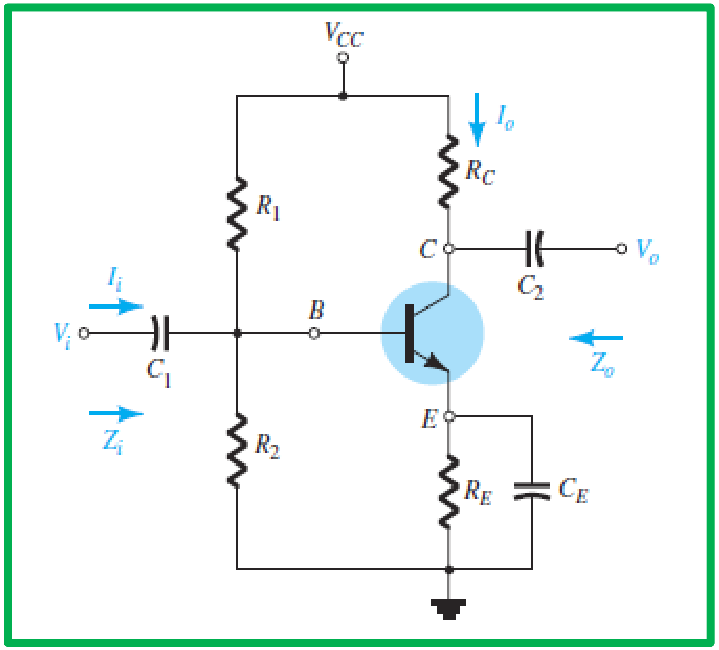


Figure 5.27: *Voltage-divider bias configuration.*

- Vividly, for the input circuit,

$$R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} \quad \textbf{[5.11]}$$

- $\boldsymbol{Z_i}$ Fig. 5.27 clearly shows that

$$Z_i = R' \| \beta r_e \ [\Omega] \quad \textbf{[5.12]}$$

- $\boldsymbol{Z_o}$ Let $V_i = 0$ so that $I_b = 0$ and $\beta I_b = 0$, thus,

$$Z_o = R_C \| r_o \ [\Omega] \quad \textbf{[5.13]}$$

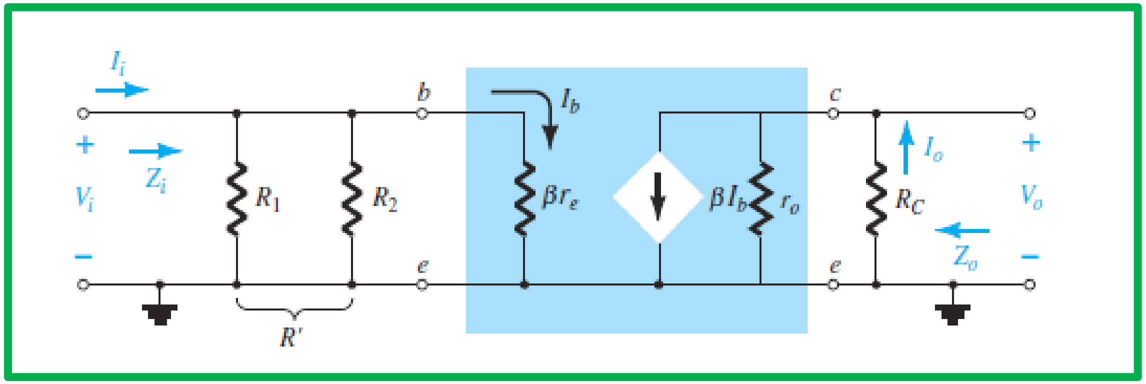


Figure 5.27: *ac equivalent of Fig. 5.27 with r_e model.*

5.6 Voltage-Divider Bias Cont'd

- For $r_o \geq 10R_C$, we have $\boxed{Z_o \cong R_C \big|_{r_o \geq 10R_C} [\Omega]}$ **[5.14]**

- $\boldsymbol{A_V}$ The voltage gain is obtained as follows,

$$V_o = -\beta I_b \left(R_C \parallel r_o\right);$$

- But $I_b = \dfrac{V_i}{\beta r_e}; \quad \Rightarrow V_o = -\beta\left(\dfrac{V_i}{\beta r_e}\right)\left(R_C \parallel r_o\right);$

- Thus,

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{\left(R_C \parallel r_o\right)}{r_e}} \quad \textbf{[5.15]}$$

- If $r_o \geq 10R_C$, so that the effect of r_o can be ignored,

$$\boxed{A_v \cong -\frac{R_C}{r_e}\bigg|_{r_o \geq 10R_C}} \quad \textbf{[5.16]}$$

Phase Relationship

- The negative sign in Eq. [5.16] reveals a 180^o phase shift between V_o and V_i.

Example 5.2 Voltage-Divider Bias Configuration

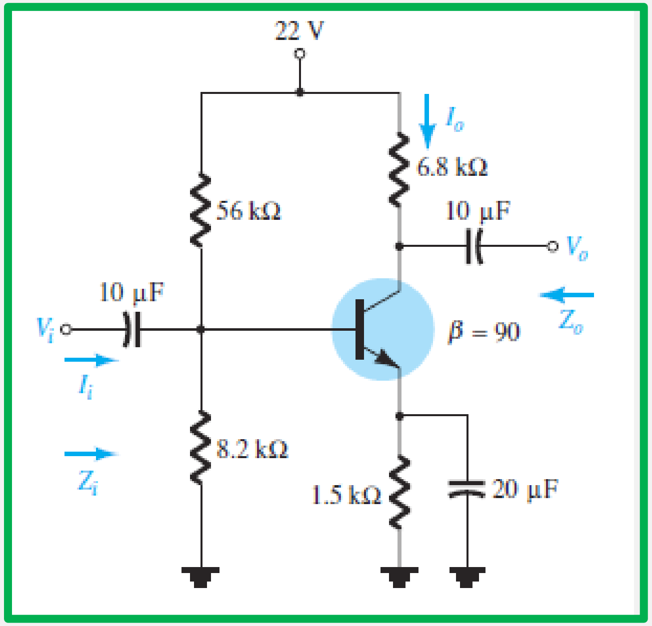


Figure 5.28: *Example 5.2.*

- For the network of Fig. 5.28, determine:
  - **a)** r_e.
  - **b)** Z_i (with $r_o = \infty\Omega$) .
  - **c)** Z_o (with $r_o = \infty\Omega$) .
  - **d)** A_v (with $r_o = \infty\Omega$) .
  - **e)** The parameters of parts (b) through (d) if $r_o = 50\,\text{k}\Omega$ and compare results.

[Solution]

a) DC: Testing $\beta R_E > 10 R_2$;

$$\Rightarrow (90)(1.5\text{k}\Omega) > 10(8.2\text{k}\Omega);\ \text{i.e.,}\ 135\text{k}\Omega > 82\text{k}\Omega$$ (Satisfied)

Using the approximate approach, yields

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{(8.2\text{k}\Omega)(22\,\text{V})}{56\text{k}\Omega + 8.2\text{k}\Omega} = 2.81\,\text{V}$$

Example 5.2 Voltage-Divider Bias Configuration Cont'd

$$V_E = V_B - V_{BE} = 2.81\,\text{V} - 0.7\,\text{V} = 2.11\,\text{V}$$

$$I_E = \frac{V_E}{R_E} = \frac{2.11\,\text{V}}{1.5\,\text{k}\Omega} = 1.41\,\text{mA}$$

$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{1.41\,\text{mA}} = \mathbf{18.44\ \Omega}$$

b) $$R' = R_1 \| R_2 = (56\,\text{k}\Omega) \| (8.2\,\text{k}\Omega) = \mathbf{7.15\,k\Omega}$$

$$Z_i = R' \| \beta r_e = 7.15\,\text{k}\Omega \| (90)(18.44\,\Omega) = 7.15\,\text{k}\Omega \| 1.66\,\text{k}\Omega = \mathbf{1.35\,k\Omega}$$

c) $$Z_o = R_C = \mathbf{6.8\,k\Omega}$$

d) $$A_v = -\frac{R_C}{r_e} = -\frac{6.8\,\text{k}\Omega}{18.44\,\Omega} = \mathbf{-368.76}$$

e) $$Z_i = \mathbf{1.35\,k\Omega}; \qquad Z_o = R_C \| r_o = 6.8\,\text{k}\Omega \| 50\,\text{k}\Omega = \mathbf{5.98\,k\Omega} \quad \text{vs}\ 6.8\,\text{k}\Omega$$

$$A_v = -\frac{r_o \| R_C}{r_e} = -\frac{5.98\,\text{k}\Omega}{18.44\,\Omega} = \mathbf{-324.3} \quad \text{vs}\ -368.76$$

5.7 CE Emitter-Bias Configuration

❑ Unbypassed

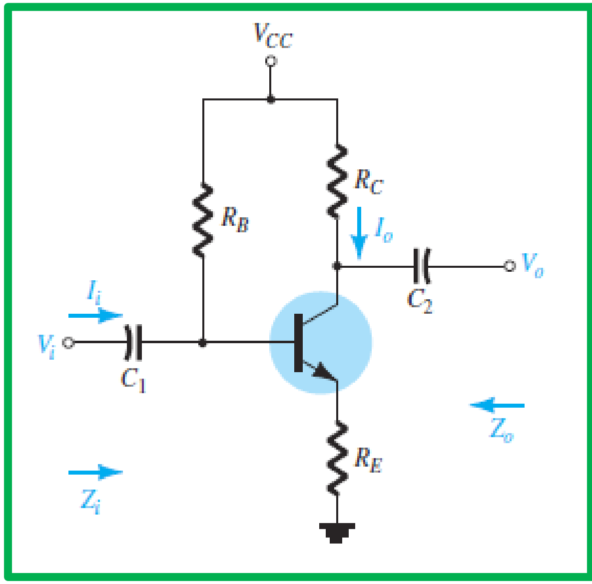


Figure 5.29: CE emitter-bias configuration.

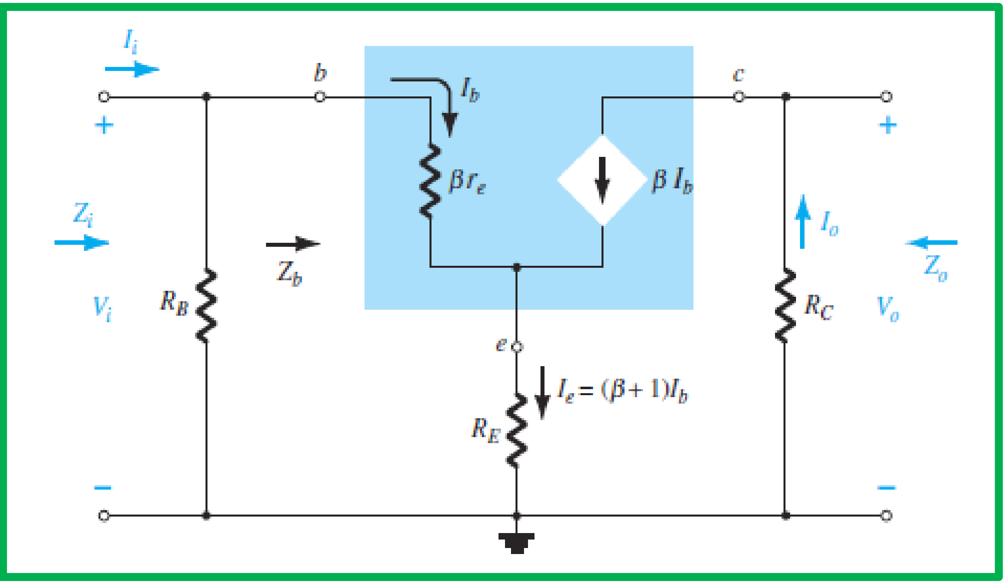


Figure 5.30: ac equivalent of Fig. 5.29 with r_e model.

- ❑ Notice that here we ignore r_o to lessen the complexity of our analysis.
- ❑ KVL applied to input side of Fig. 5.30 gives, $V_i = I_b \beta r_e + I_e R_E$;

$$\Rightarrow V_i = I_b \beta r_e + (\beta + 1) I_b R_E \; ; \quad \therefore Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1) R_E$$

5.7 CE Emitter-Bias Configuration Cont'd

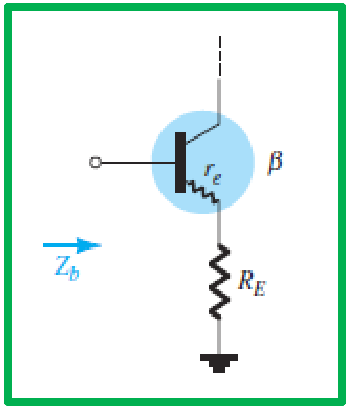


Figure 5.31: *Defining input impedance of CE with unbypassed R_E.*

- Clearly, the impedance of a transistor with unbypassed resistor R_E is determined by

$$\boxed{Z_b = \beta r_e + (\beta + 1) R_E} \qquad \textbf{[5.17]}$$

- Its approximation is thus,

$$Z_b \cong \beta r_e + \beta R_E$$

$$\boxed{Z_b \cong \beta (r_e + R_E)} \qquad \textbf{[5.18]}$$

- Most often $R_E \gg r_e$ as such further approximation is

$$\boxed{Z_b \cong \beta R_E} \qquad \textbf{[5.19]}$$

- $\boldsymbol{Z_i}$ Fig. 5.30 clearly gives $\boxed{Z_i = R_B \| Z_b \ [\Omega]}$ **[5.20]**

- $\boldsymbol{Z_o}$ Let $V_i = 0$ so that $I_b = 0$ and $\beta I_b = 0$, thus,

$$\boxed{Z_o = R_C \ [\Omega]} \qquad \textbf{[5.21]}$$

5.7 CE Emitter-Bias Configuration Cont'd

- A_V The voltage gain is obtained as follows,

$$I_b = \frac{V_i}{\beta r_e}\ ; \quad V_o = -I_o R_C = -\beta I_b R_C\ ; \quad \Rightarrow V_o = -\beta\left(\frac{V_i}{Z_b}\right)R_C\ ;$$

- Thus,

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b}} \qquad [5.22]$$

- Substituting $Z_b \cong \beta(r_e + R_E)$ yields,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e + R_E}} \qquad [5.23]$$

- Furthermore, for the approximation $Z_b \cong \beta R_E$ we have,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{R_E}} \qquad [5.24]$$

Phase Relationship

- The negative sign in Eq. [5.16] reveals a 180^{o} phase shift between V_o and V_i .

5.7 CE Emitter-Bias Configuration Cont'd

- **Effect of r_o** We list these complex equations without deriving them,
- Z_i

$$Z_b = \beta r_e + \left[\frac{(\beta+1) + R_C/r_o}{1+(R_C+R_E)/r_o}\right] R_E \qquad [5.25]$$

- An approximation is obtained for $r_o \geq 10(R_C+R_E)$ and $\beta+1 \cong \beta$,

$$Z_b \cong \beta(r_e+R_E)\Big|_{r_o \geq 10(R_C+R_E)} \qquad [5.26]$$

- Z_o

$$Z_o = R_C \left\| \left[r_o + \frac{\beta(r_o+r_e)}{1+(\beta r_e/R_E)} \right] \right. \qquad [5.27]$$

- Its approximation based on $r_o \gg r_e$ is thus,

$$Z_o \cong R_C \quad [\Omega] \qquad [5.28]$$

- A_v

$$A_v = \frac{V_o}{V_i} = \frac{-(\beta R_C/Z_b)\left[1+(r_e/r_o)\right]+(R_C/r_o)}{1+(R_C/r_o)} \qquad [5.29]$$

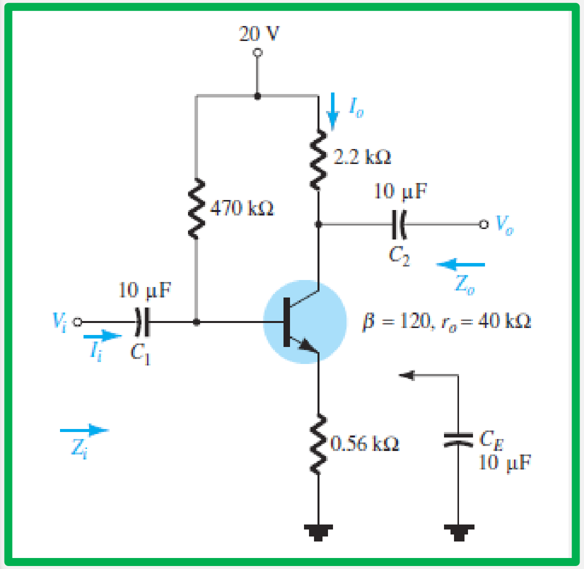
5.7 CE Emitter-Bias Configuration Cont'd

- For $r_o \geq 10R_C$,

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b}\bigg|_{r_o \geq 10R_C}} \quad [5.30]$$

- **Bypassed**
- Notice that we have looked at this in section 5.5 and Eqs [5.5] to [5.6] apply.

Example 5.3 CE Emitter-Bias Configuration



- For the network of Fig. 5.32, without C_E (unbypassed), determine:

a) r_e.

b) Z_i .

c) Z_o .

d) A_v .

Figure 5.32: Example 5.3.

[Example 5.3] CE Emitter-Bias Configuration Cont'd

[Solution]

a) DC: $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_E} = \frac{20\,\text{V} - 0.7\,\text{V}}{470\,\text{k}\Omega + (121)(0.56\,\text{k}\Omega)} = 35.89\,\mu\text{A}$$

$$I_E = (\beta+1)I_B = (121)(35.89\,\mu\text{A}) = 4.34\,\text{mA}$$

$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{4.34\,\text{mA}} = \mathbf{5.99\ \Omega}$$

b) Testing the condition $r_o \geq 10(R_C + R_E)$, we have

$$40\,\text{k}\Omega \geq 10(2.2\,\text{k}\Omega + 0.56\,\text{k}\Omega)$$

$$40\,\text{k}\Omega \geq 10(2.76\,\text{k}\Omega) = 27.6\,\text{k}\Omega \qquad \text{(Satisfied)}$$

$$Z_b \cong \beta(r_e + R_E) = 120(5.99\Omega + 560\Omega) = 67.92\,\text{k}\Omega$$

$$Z_i = R_B \| Z_b = 470\,\text{k}\Omega \| 67.92\,\text{k}\Omega = \mathbf{59.34\,k\Omega}$$

c) $$Z_o = R_C = \mathbf{2.2\,k\Omega}$$

[Example 5.3] CE Emitter-Bias Configuration Cont'd

d) $r_o \geq 10R_C$ is satisfied. Therefore,

$$A_v = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b} = -\frac{(120)(6.8\,\text{k}\Omega)}{67.92\,\text{k}\Omega} = \mathbf{-3.89}$$ (a relatively low gain indeed)

- Compared to -3.93 using Eq. [5.20]: $A_v \cong -R_C/R_E$.

[Example 5.4] CE Emitter-Bias Configuration

- Repeat the analysis of Example 5.3 with C_E in place.

[Solution] **a)** The dc analysis is the same, and $r_e = \mathbf{5.99\ \Omega}$

b) R_E is "shorted out" by C_E for ac analysis. Therefore,

$$Z_i = R_B \| Z_b = R_B \| \beta r_e = 470\,\text{k}\Omega \| (120)(5.99\,\Omega) = \mathbf{717.70\Omega}$$

c) $Z_o = R_C = \mathbf{2.2k\Omega}$

d) $$A_v = -\frac{R_C}{r_e} = -\frac{2.2\,\text{k}\Omega}{5.99\,\Omega} = \mathbf{-367.28}$$ (a huge increase)

5.8 Emitter-Follower Configuration

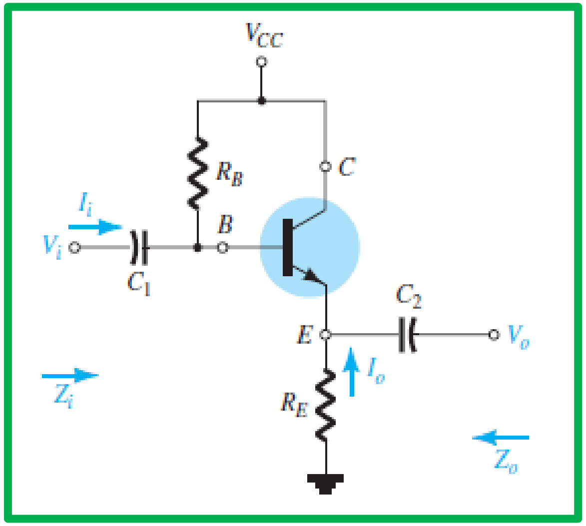


Figure 5.33: *Emitter-follower configuration.*

- The fact that V_o "follows" the magnitude of V_i with an in-phase relationship accounts for the terminology emitter-follower.

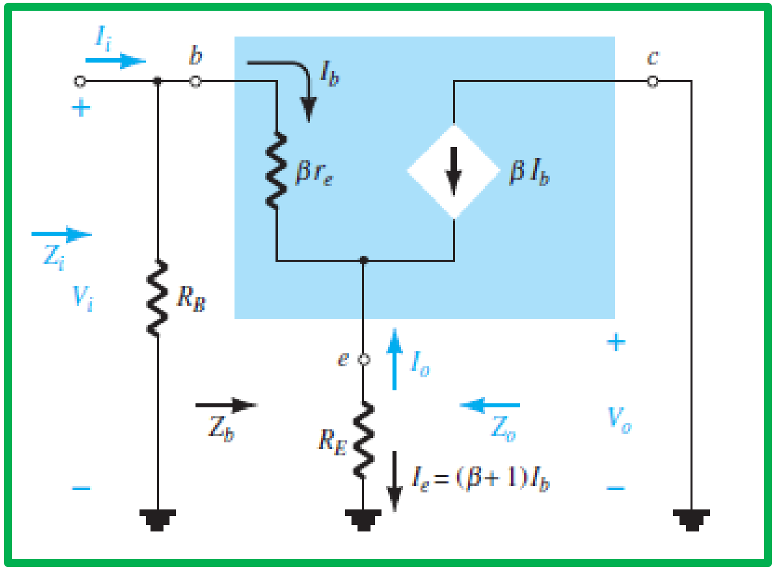


Figure 5.34: *ac equivalent of Fig. 5.33 with r_e model.*

- $\boldsymbol{Z_i}$ Fig. 5.33 clearly gives

$$Z_i = R_B \| Z_b \quad [\Omega] \qquad [5.31]$$

- with

$$Z_b = \beta r_e + (\beta + 1) R_E \qquad [5.32]$$

- Its approximation is thus,

$$Z_b \cong \beta (r_e + R_E) \qquad [5.33]$$

5.8 Emitter-Follower Configuration Cont'd

- Further approximation is $$\boxed{Z_b \cong \beta R_E \Big|_{R_E \gg r_e}}$$ **[5.34]**

- ***Z*$_o$** The output impedance is found as follows

$$I_b = \frac{V_i}{Z_b} \;; \quad \text{such that} \quad I_e = (\beta+1) I_b = (\beta+1)\frac{V_i}{Z_b} \;;$$

- Substituting for Z_b gives

$$I_e = \frac{(\beta+1)V_i}{\beta r_e + (\beta+1)R_E} \;; \quad \text{that is,} \quad I_e = \frac{V_i}{\left[\beta r_e/(\beta+1)\right] + R_E}$$

- Notice that for $(\beta+1) \cong \beta \;; \quad \Rightarrow \quad \dfrac{\beta r_e}{\beta+1} \cong \dfrac{\beta r_e}{\beta} = r_e$

- Thus, $$\boxed{I_e \cong \frac{V_i}{r_e + R_E}}$$ **[5.35]**

5.8 Emitter-Follower Configuration Cont'd

- If we now construct the network defined by Eq. [5.35] , Fig. 5.35 results.

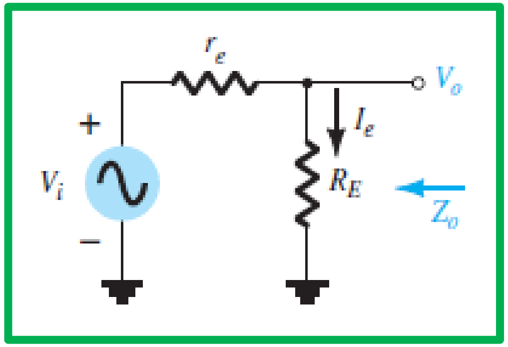


Figure 5.35: Defining Z_o for emitter-folower

- ***Z_o*** Let $V_i = 0$ so that,

$$\boxed{Z_o = R_E \| r_e \ \ [\Omega]} \qquad [5.36]$$

- Its approximation based on $R_E \gg r_e$ is thus,

$$\boxed{Z_o \cong r_e \ \ [\Omega]} \qquad [5.37]$$

- ***A_v*** Voltage gain is determined through exploitation of voltage-divider, i.e.,

$$V_o = \frac{R_E V_i}{R_E + r_e} \ ; \quad \Rightarrow \quad \boxed{A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e}} \qquad [5.38]$$

- Typically $R_E \gg r_e$ thus $R_E + r_e \cong R_E$, so that

$$\boxed{A_v = \frac{V_o}{V_i} \cong 1} \qquad [5.39]$$

5.8 Emitter-Follower Configuration Cont'd

Phase Relationship

- Vividly Eq. 5.38 has revealed that V_i and V_o are in phase.

Effect of r_o

- Z_i

$$\boxed{Z_b = \beta r_e + \frac{(\beta+1)R_E}{1+R_E/r_o}} \qquad [5.40]$$

- If $r_o \geq 10R_E$ is satisfied, $Z_b = \beta r_e + (\beta+1)R_E$
- This matches

$$\boxed{Z_b \cong \beta(r_e + R_E)\Big|_{r_o \geq 10R_E}} \qquad [5.41]$$

- Z_o

$$\boxed{Z_o = r_o \| R_E \| \frac{\beta r_e}{(\beta+1)} \; [\Omega]} \qquad [5.42]$$

- For $(\beta+1) \cong \beta$, $Z_o = r_o \| R_E \| r_e \; [\Omega]$
- For $r_o \gg r_e$,

$$\boxed{Z_o = R_E \| r_e \; [\Omega]} \qquad [5.43]$$

5.8 Emitter-Follower Configuration Cont'd

- A_V

$$\boxed{A_V = \frac{(\beta+1)R_E/Z_b}{1+R_E/r_o}} \quad [5.44]$$

- If $r_o \geq 10R_E$ is satisfied and we use the approximation $(\beta+1) \cong \beta$, we find

$$A_V \cong \frac{\beta R_E}{Z_b}$$

- But

$$Z_b \cong \beta(r_e + R_E)\Big|_{r_o \geq 10R_E}$$

- So that,

$$A_V \cong \frac{\beta R_E}{\beta(r_e + R_E)}$$

- This yields,

$$\boxed{A_V \cong \frac{R_E}{(r_e + R_E)}\Bigg|_{r_o \geq 10R_E}} \quad [5.45]$$

5.9 Common-Base Configuration

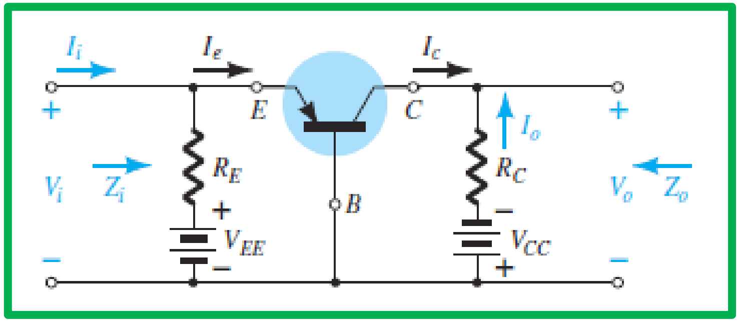
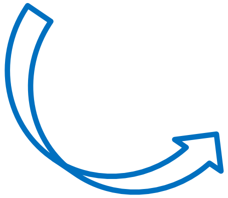


Figure 5.36: Common-base configuration.

- The CB has relatively low input and high output impedance and a current gain less than 1.



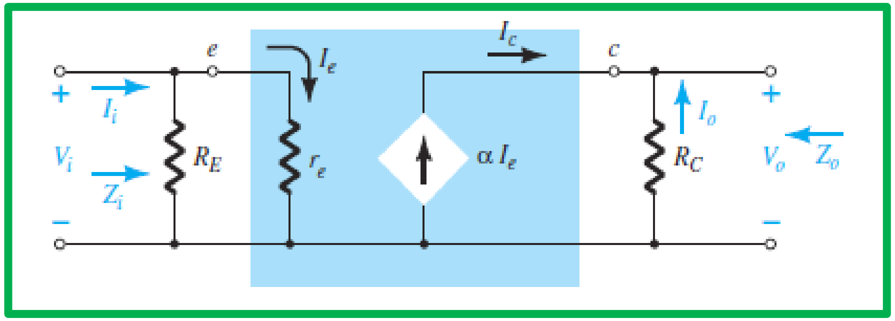


Figure 5.37: ac equivalent of Fig. 5.36 with r_e model.

- Z_i Fig. 5.33 clearly gives

$$\boxed{Z_i = R_E \| r_e \ \ [\Omega]} \qquad [5.46]$$

- Z_o

$$\boxed{Z_o = R_C \ \ [\Omega]} \qquad [5.47]$$

- A_V

$$V_o = -I_o R_C = -(-I_c) R_C = \alpha I_e R_C$$

5.9 Common-Base Configuration Cont'd

- With $I_e = \dfrac{V_i}{r_e}$ so that, $V_o = \alpha\left(\dfrac{V_i}{r_e}\right)R_C$

- Thus

$$\boxed{A_V = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e}} \qquad [5.48]$$

- A_i Assuming that $R_E \gg r_e$ yields

$I_e = I_i$ and that, $I_o = -\alpha I_e = -\alpha I_i$

- Thus,

$$\boxed{A_i = \frac{I_o}{I_i} = -\alpha \cong -1} \qquad [5.49]$$

Phase Relationship

- Vividly Eq. 5.48 shows that A_V is positive hence V_i and V_o are in phase.

Effect of r_o

- For CB, $r_o = 1/h_{ob}$ is typically in mega-ohm range, thus $r_o \| R_C \cong R_C$.

[Example 5.4] Common-Base Configuration

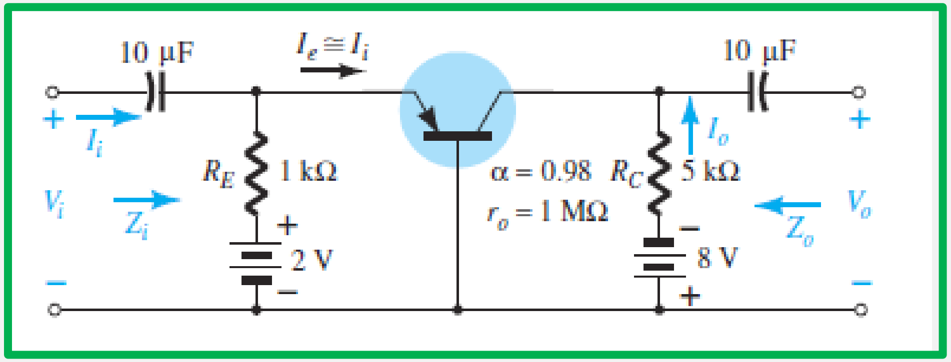


Figure 5.38: Example 5.4.

- For the network of Fig. 5.38, determine:

a) r_e .

b) Z_i .

c) Z_o .

d) A_v .

e) A_i .

[Solution]

a) DC: $$I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{2\,\text{V} - 0.7\,\text{V}}{1\,\text{k}\Omega} = 1.3\,\text{mA}$$

$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{1.3\,\text{mA}} = \mathbf{20\ \Omega}$$

b) $$Z_i = R_E \| r_e = 1\,\text{k}\Omega \| 20\,\Omega = \mathbf{19.61\,\Omega} \cong r_e$$

c) $$Z_o = R_C = \mathbf{5\,k\Omega}$$

d) $$A_V \cong \frac{R_C}{r_e} = \frac{5\,\text{k}\Omega}{20\,\Omega} = \mathbf{250}$$

e) $$A_i = -0.98 \cong -1$$

5.10 Cascaded Systems

- The two-port systems approach is particularly useful for cascaded systems.

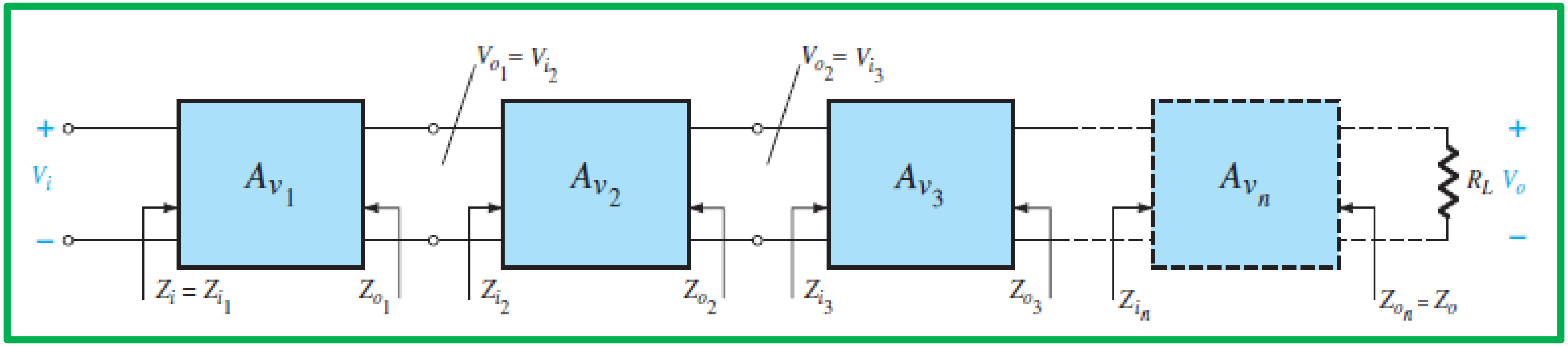


Figure 5.39: Cascaded system.

- In Fig. 5.39 $A_{v_1}, A_{v_2}, A_{v_3}, \cdots, A_{v_n}$ are voltage gains of each stage under loaded conditions.
- That is, A_{v_1} is determined with the input impedance to A_{v_2} acting as the load on A_{v_1}.
- For A_{v_2}, A_{v_1} will determine the signal strength and source impedance at the input to A_{v_2}. The total gain of the system is of the form

$$\boxed{A_{v_T} = A_{v_1} A_{v_2} A_{v_3} \cdots A_{v_n}} \qquad [5.50]$$

5.10 Cascaded Systems Cont'd

- The total current gain is given by

$$\boxed{A_{i_T} = -A_{v_T}\frac{Z_{i_1}}{R_L}} \qquad [5.51]$$

- Note that, no matter how perfect the system design, the application of a succeeding stage or load to a two-port system will affect the voltage gain.
- Thus, $A_{v_1}, A_{v_2}, A_{v_3}, \cdots, A_{v_n}$ cannot be simply the **no-load values** $A_{v_1,\mathrm{NL}}, A_{v_2,\mathrm{NL}},$ and so forth.

[Example 5.5] Cascaded Systems

- The two-stage system of Fig. 5.40 employs a transistor emitter-follower configuration prior to a common-base configuration to ensure that the maximum percentage of applied signal appears at the input terminals of the common-base amplifier.

[Example 5.5] Cascaded Systems Cont'd

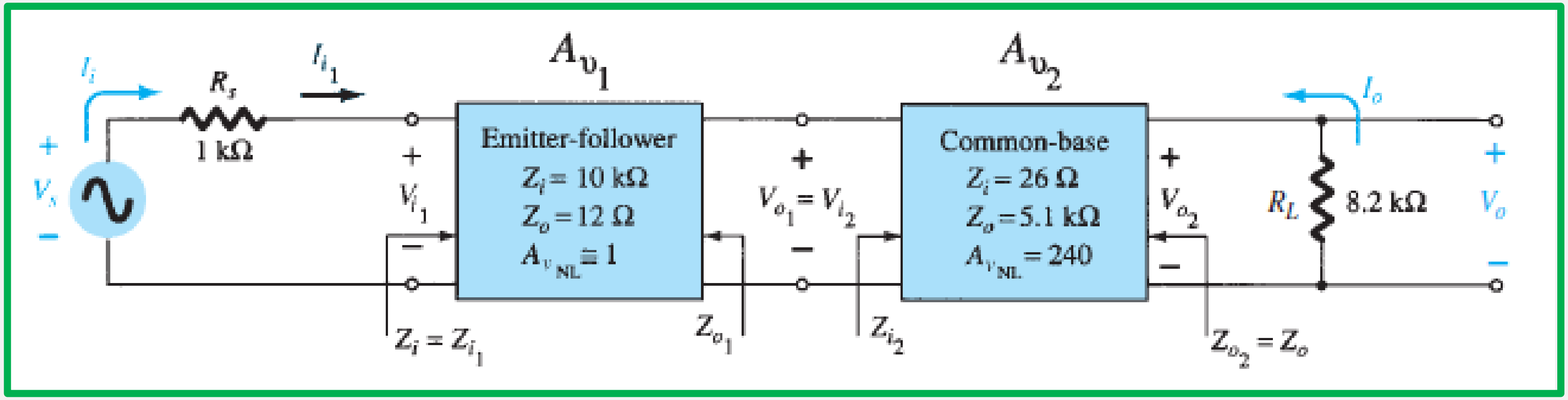


Figure 5.40: Example 5.5.

- In Fig. 5.40, the no-load (NL) values are provided for each system, with the exception of Z_i and Z_o for the emitter-follower, which are the loaded values. For the system of Fig. 5.40, determine:

a) The loaded gain for each stage.

b) The total gain for the system, A_v and A_{v_s} .

c) The total current gain for the system.

d) The total gain for the system if the emitter-follower system were removed.

[Example 5.5] Cascaded Systems Cont'd

[Solution]

a) For the emitter-follower, the loaded gain is

$$V_{o_1} = \frac{Z_{i_2}}{Z_{i_2} + Z_{o_1}} A_{v_{NL}} V_{i_1} = \frac{26\Omega}{26\Omega + 12\Omega}(1) V_{i_1} = 0.684 V_{i_1}$$

- Thus $A_{v_1} = \dfrac{V_{o_1}}{V_{i_1}} = \mathbf{0.684}$

- For the common-base configuration,

$$V_{o_2} = \frac{R_L}{R_L + R_{o_2}} A_{v_{NL}} V_{i_2} = \frac{8.2\,\text{k}\Omega}{8.2\,\text{k}\Omega + 5.1\,\text{k}\Omega}(240) V_{i_2} = 147.97 V_{i_2}$$

- Thus $A_{v_2} = \dfrac{V_{o_2}}{V_{i_2}} = \mathbf{147.97}$

b) Eq. [5.50]: $A_{v_T} = A_{v_1} A_{v_2} = (0.684)(147.97) = \mathbf{101.20}$

[Example 5.5] Cascaded Systems Cont'd

- The voltage gain for the entire system with source resistance included is

$$V_{o_2} = \frac{Z_{i_1}}{Z_{i_1} + R_s} V_s A_{v_T} \quad ;$$

$$\Rightarrow A_{v_s} = \frac{V_{o_2}}{V_s} = \frac{Z_{i_1}}{Z_{i_1} + R_s} A_{v_T} = \frac{10\,\text{k}\Omega}{10\,\text{k}\Omega + 1\,\text{k}\Omega}(101.20) = \mathbf{92}$$

c) Total current gain for Eq. [5.51]

$$A_{i_T} = -A_{v_T} \frac{Z_{i_1}}{R_L} = -(101.20)\left(\frac{10\,\text{k}\Omega}{8.2\,\text{k}\Omega}\right) = \mathbf{-123.41}$$

- Alternatively, $I_{i_1} = \frac{V_s}{R_s + Z_{i_1}}$; $I_{o_2} = -\frac{V_{o_2}}{R_L}$;

$$A_{i_T} = \frac{I_{o_2}}{I_{i_1}} = -A_{v_s} \frac{R_s + Z_{i_1}}{R_L} = -(92)\left(\frac{1\,\text{k}\Omega + 10\,\text{k}\Omega}{8.2\,\text{k}\Omega}\right) = \mathbf{-123.41}$$

[Example 5.5] Cascaded Systems Cont'd

d) If the emitter follower is removed, the source directly applies the signal to the common-base system.

$$V_i = \frac{Z_{i_{\text{CB}}}}{Z_{i_{\text{CB}}} + R_s} V_s = \frac{26\,\Omega}{26\,\Omega + 1\,\text{k}\Omega} V_s = 0.025 V_s \quad ;$$

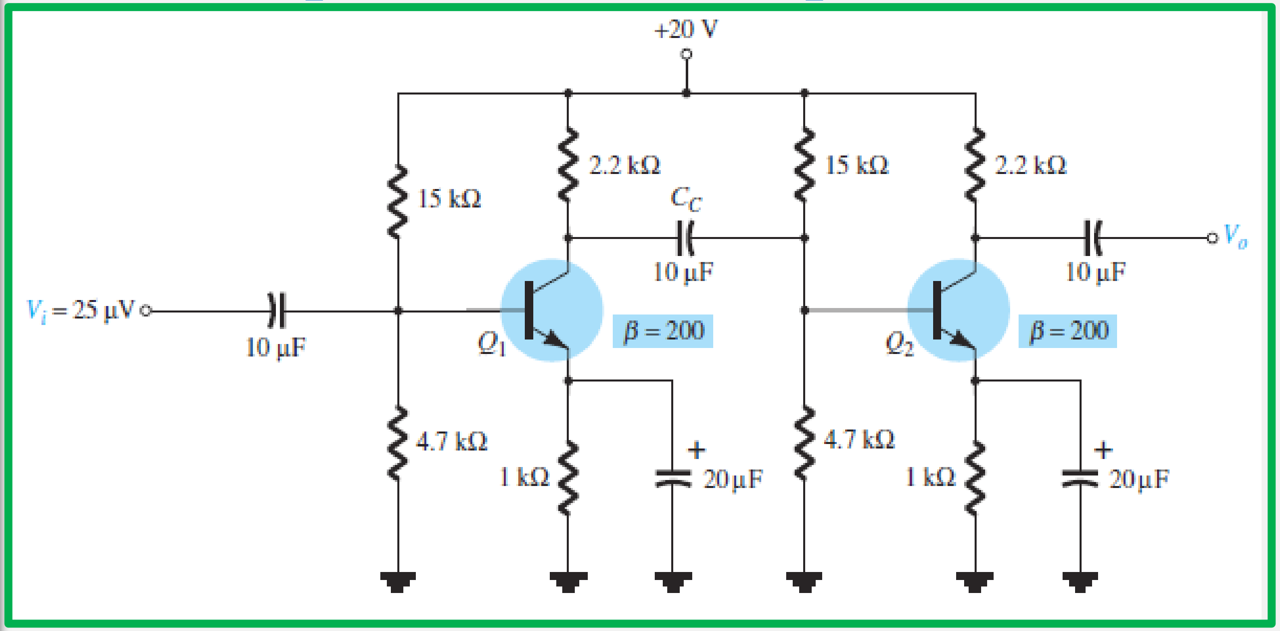
- So that $\dfrac{V_i}{V_s} = 0.025$ with $\dfrac{V_o}{V_i} = 147.97$ from above
- Thus $A_{v_s} = \dfrac{V_o}{V_s} = \left(\dfrac{V_i}{V_s}\right)\left(\dfrac{V_o}{V_i}\right) = (0.025)(147.97) = \mathbf{3.7}$
- Notice that the total gain is about 25 times greater with the emitter-follower system.
- It is worth noting that the output impedance of the first stage is relatively close to the input impedance of the second stage, otherwise the signal would have been "lost" again by voltage divider action.

5.10 Cascaded Systems

RC-Coupled BJT Amplifiers

- The Coupling capacitor isolates the two stages from dc viewpoint but acts as short-circuit for the ac response.
- Input impedance of second stage acts as a load on first stage, thus approach used earlier applies.

[Example 5.6] Cascaded Systems



a) Calculate the no-load gain and V_o .

b) Calculate the overall gain and V_o if load is $R_L = 4.7\,\text{k}\Omega$, compare to the results of part (a).

c) Calculate Z_{i_1} and Z_{o_2} .

Figure 5.41: Example 5.6.

[Example 5.6] Cascaded Systems Cont'd

[Solution]

a) The dc bias analysis yields the following for each BJT

$$V_B = 4.8\,\text{V}\ ; \quad V_E = 4.1\,\text{V}\ ; \quad V_C = 11\,\text{V}\ ; \quad I_E = 4.1\,\text{mA}$$

- At the Q-point
$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{4.1\,\text{mA}} = 6.34\,\Omega$$

- Thus, the loading of the second stage is, $Z_{i_2} = R_1 \| R_2 \| \beta r_e$

$$\Rightarrow A_{v_1} = -\frac{R_C \| \left(R_1 \| R_2 \| \beta r_e\right)}{r_e} = -\frac{(2.2\,\text{k}\Omega) \| \left[15\,\text{k}\Omega \| 4.7\,\text{k}\Omega_1 \| (200)(6.34\,\Omega)\right]}{6.34\,\Omega}$$

$$\therefore\ A_{v_1} = -\frac{659.2\,\Omega}{6.34\,\Omega} = -104$$

- For the unloaded second stage the gain is $A_{v_2(\text{NL})} = -\dfrac{R_C}{r_e} = \dfrac{2.2\,\text{k}\Omega}{6.34\,\Omega} = -347$

- The overall gain is thus, $A_{v_T(\text{NL})} = A_{v_1} A_{v_2(\text{NL})} = -(104)(-347) \cong \mathbf{36.1 \times 10^3}$

- The output voltage is, $V_o = A_{v_T(\text{NL})} V_i = \left(36.1 \times 10^3\right)(25\,\mu\text{V}) \cong \mathbf{902.5\,mV}$

[Example 5.6] Cascaded Systems Cont'd

b) The overall gain with the $R_L = 4.7\,\text{k}\Omega$ load applied to the second stage is

$$A_{v_T} = \frac{V_o}{V_i} = \frac{R_L}{R_L + Z_o} A_{v_T(\text{NL})} = \frac{4.7\,\text{k}\Omega}{4.7\,\text{k}\Omega + 2.2\,\text{k}\Omega}\left(36.1\times 10^3\right) \cong \mathbf{24.6\times 10^3}$$

- This gain is considerably less than the $A_{v_T(\text{NL})} \cong \mathbf{36.1\times 10^3}$ because R_L is relatively close to R_C .
- Furthermore, $V_o = A_{v_T} V_i = \left(24.6\times 10^3\right)\left(25\,\mu\text{V}\right) = \mathbf{615\,mV}$

c) The input impedance of the first stage is

$$Z_{i_1} = R_1 \| R_2 \| \beta r_e = 15\,\text{k}\Omega \| 4.7\,\text{k}\Omega_1 \| (200)(6.34\,\Omega) = \mathbf{0.94\,k\Omega}$$

- Where as the output impedance for the second stage is,

$$Z_{o_2} = R_C = \mathbf{2.2\,k\Omega}$$

5.11 The Hybrid Equivalent Model

- The r_e model has the advantage that the parameters are defined by actual operating conditions.
- On the contrary, the parameters of the hybrid equivalent circuit are defined in general terms for any operating conditions.
- Notice that all specification sheets provide hybrid parameters and it is up to the designer to convert them to a particular model, say r_e model.

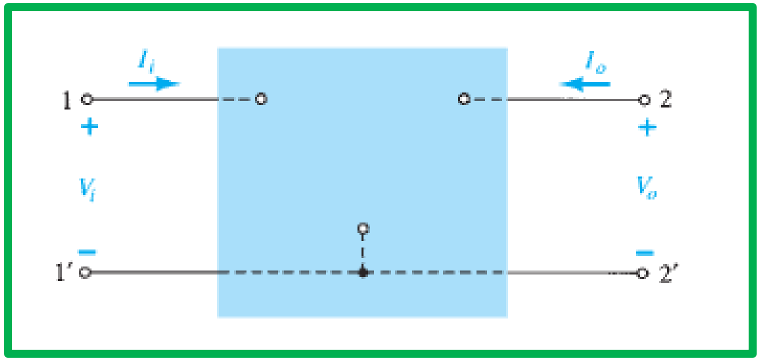


Figure 5.42: Two-port system.

- The description of the hybrid equivalent model will begin with the two-port system of Fig. 5.42.

$$V_i = h_{11} I_i + h_{12} V_o \quad [5.52]$$

$$I_o = h_{21} I_i + h_{22} V_o \quad [5.53]$$

- Thus, the *h-parameters* relate variables *V* and *I*. This is based on the term *hybrid* which was chosen because of the mixture of variables (*V* and *I*) in each equation.

5.11 The Hybrid Equivalent Model Cont'd

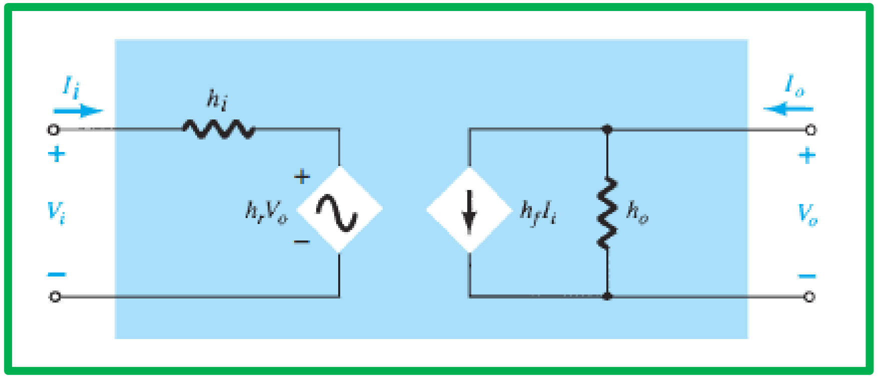
- Thus, the h-parameters are determined as follows:

$$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o=0} \quad \text{[ohms]} \qquad h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i=0} \quad \text{[unitless]}$$

$$h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0} \quad \text{[unitless]} \qquad h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i=0} \quad \text{[siemens]}$$

[5.54]

- This results into a complete hybrid equivalent model of Fig. 5.43.



$h_{11} \rightarrow$ input resistance $\rightarrow h_i$

$h_{12} \rightarrow$ reverse transfer voltage ratio $\rightarrow h_r$

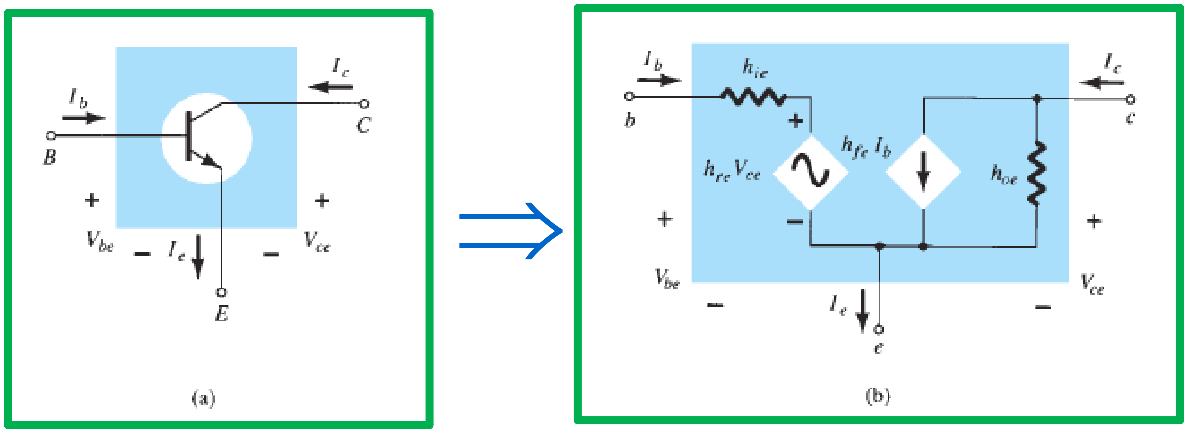
$h_{21} \rightarrow$ forward transfer current ratio $\rightarrow h_f$

$h_{22} \rightarrow$ output conductance $\rightarrow h_o$

Figure 5.43: Complete hybrid equivalent ckt.

5.11 The Hybrid Equivalent Model Cont'd

❑ Common-Emitter Configuration

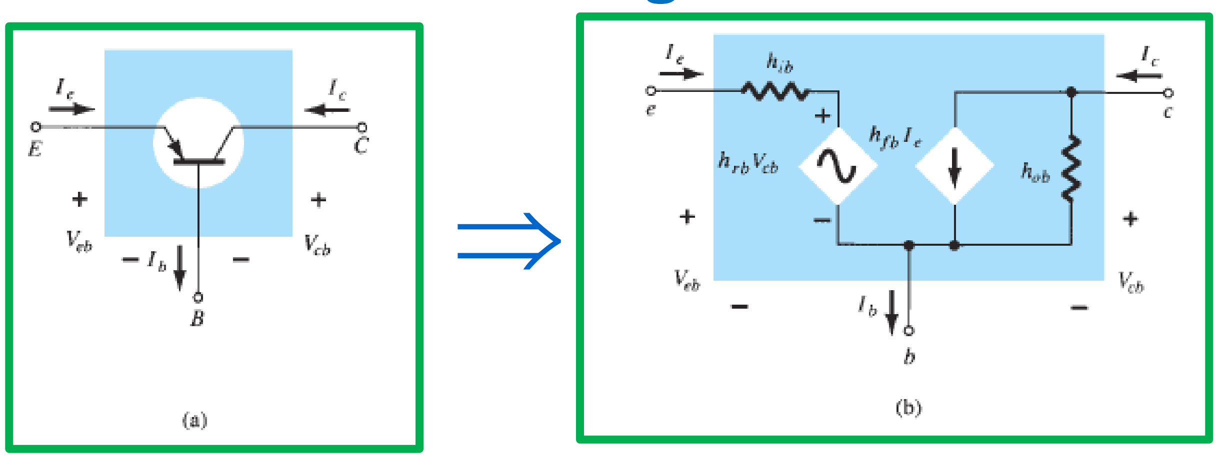


❑ Extending the hybrid equivalent model to various BJT configurations yields

Figure 5.44: CE (a) symbol; (b) Hybrid Equivalent circuit.

❑ Common-Base Configuration

Figure 5.45: CB (a) symbol; (b) Hybrid Equivalent circuit.

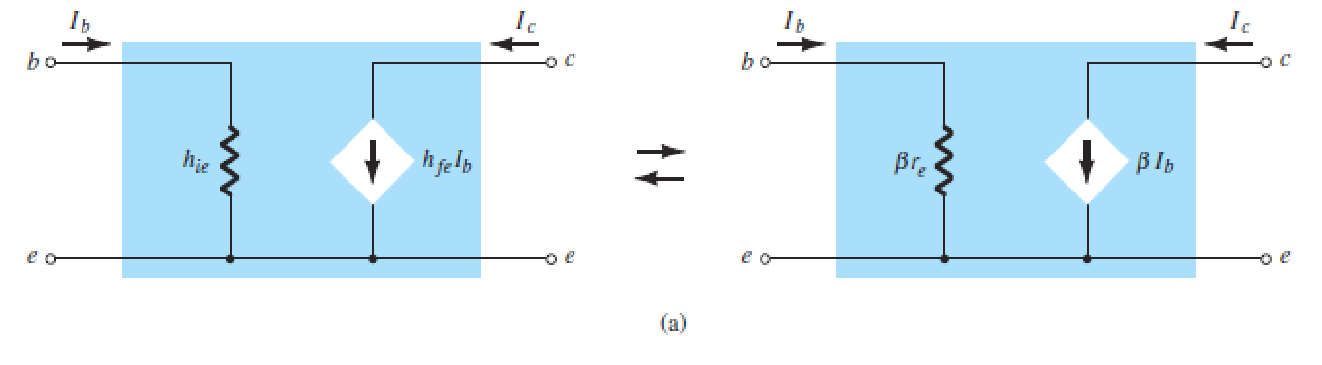


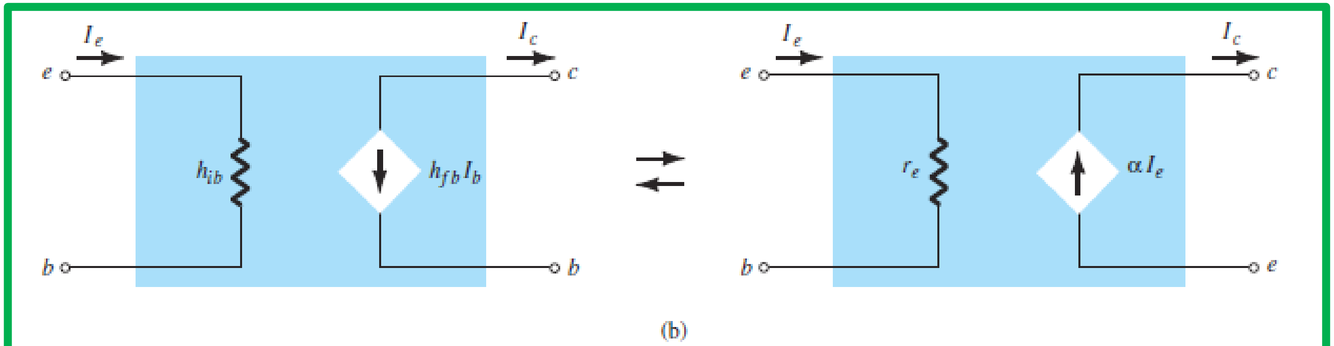
5.11 The Hybrid Equivalent Model Cont'd

- Note that h_r is normally a relatively small quantity is typically approximated by $h_r \cong 0$ and $h_r V_o \cong 0$, resulting in a short-circuit.
- Similarly, $1/h_o$ is often large enough to be ignored in comparison to a parallel load.
- Vividly,

$$\boxed{h_{ie} = \beta r_e} \quad [5.55]$$

$$\boxed{h_{fe} = \beta_{ac}} \quad [5.56]$$





$$\boxed{h_{ib} = r_e} \quad [5.57]$$

$$\boxed{h_{fb} = -\alpha \cong -1} \quad [5.58]$$

Figure 5.45: *Hybrid* versus r_e model: (a) CE; (b) CB.

5.12 Approximate Hybrid Equivalent Model

❑ Fixed-Bias Configuration

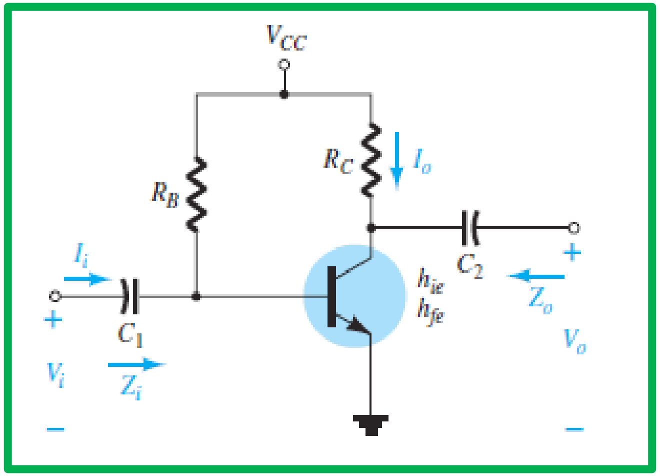


Figure 5.46: Fixed-bias configuration.

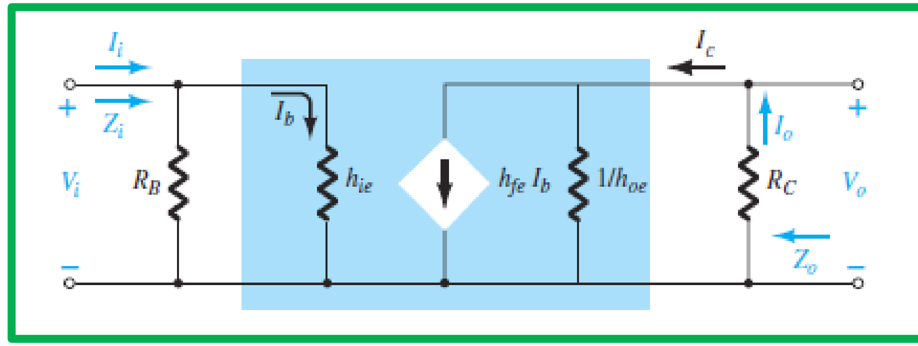


Figure 5.47: Substituting *approximate Hybrid model* into the ac equivalent network.

❑ Analysing the to determine Z_i, Z_o, A_v and A_i circuit like we did for the r_e *model* yields,

$$Z_i = R_B \| h_{ie} \quad [\Omega] \qquad [5.59]$$

$$Z_o = R_C \| 1/h_{oe} \quad [\Omega] \qquad [5.60]$$

$$A_v = \frac{V_o}{V_i} = \frac{h_{ie}\left(R_C \| 1/h_{oe}\right)}{h_{ie}} \qquad [5.61]$$

$$A_v = \frac{I_o}{I_i} \cong h_{fe}\Big|_{R_B \gg h_{ie};\ 1/h_{oe} \geq 10 R_C} \qquad [5.62]$$

5.13 Hybrid π Model

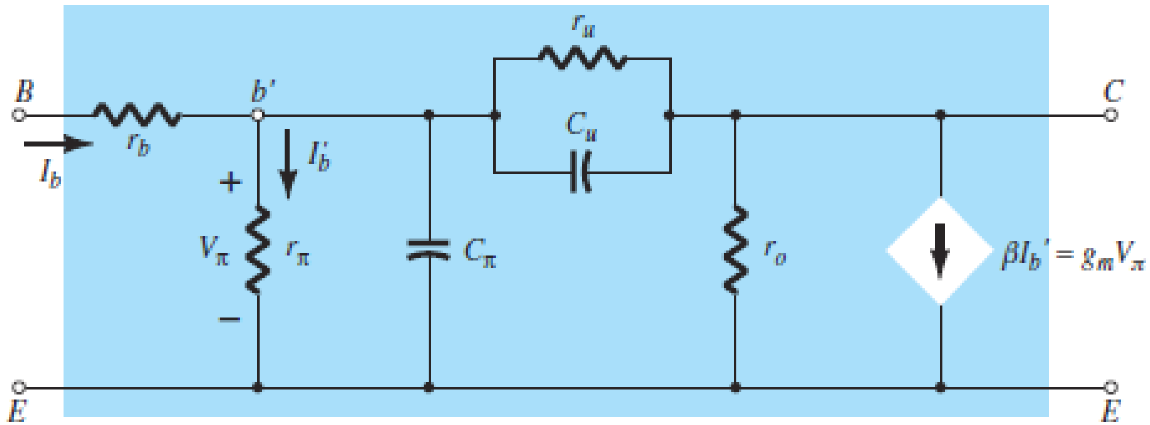


Figure 5.48: Giacoletto (or *hybrid* π) high-frequency transistor small-signal ac equivalent circuit.

- The last BJT model we are looking at is the Hybrid π model which includes parameters that are not present in the other two models discussed thus far.

r_π, r_o, r_b and r_u

- The resistors r_π, r_o, r_b and r_u are the resistances between the indicated terminals of the device when in the active region. Thus, like in the r_e *model*,

$$r_\pi = \beta r_e \quad [5.63]$$

- The resistance r_u (with subscript *u* meaning union) provides feedback path from output to input circuits, and is typically very large.

5.13 Hybrid π Model Cont'd

C_π and C_u

- All capacitors that appear in Fig. 5.48 are stray parasitic capacitors between the various junctions of the device.
- Notice that for low to mid-frequencies their reactance is very large, and they are considered open circuit.

$\beta I_b'$ or $g_m V_\pi$

- Note that the controlled source can be either a voltage-controlled current source (VCCS) or current-controlled current source (CCCS), depending on the parameters used.
- The parameter equivalence is:

$$g_m = \frac{1}{r_e} \quad [5.64]$$

$$\frac{r_\pi}{r_\pi + r_u} \cong \frac{r_\pi}{r_u} \cong h_{re} \quad [5.66]$$

$$r_o = \frac{1}{h_{oe}} \quad [5.65]$$

5.14 Variations of BJT Parameters

- A variety of curves can be drawn to show the variations of the transistor parameters with temperature, frequency, voltage and current.
- The most important at developmental stage is variations with junction temperature, collector voltage and current.

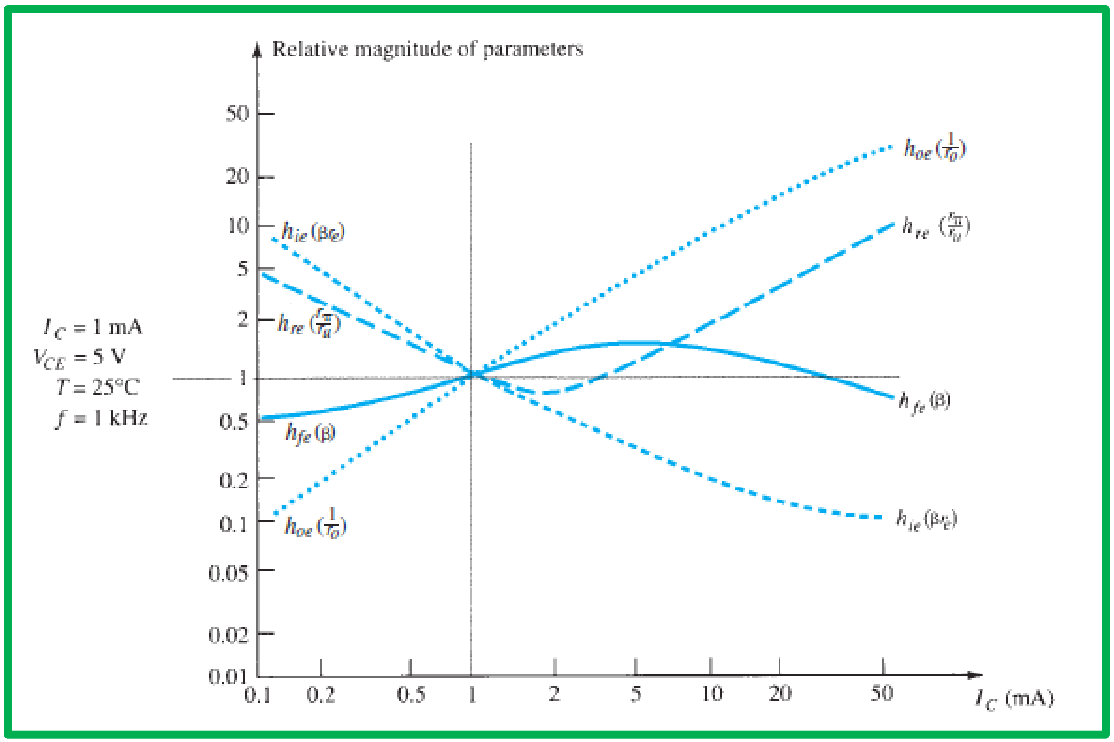


Figure 5.49: Hybrid parameter variations with collector current.

5.14 Variations of BJT Parameters Cont'd

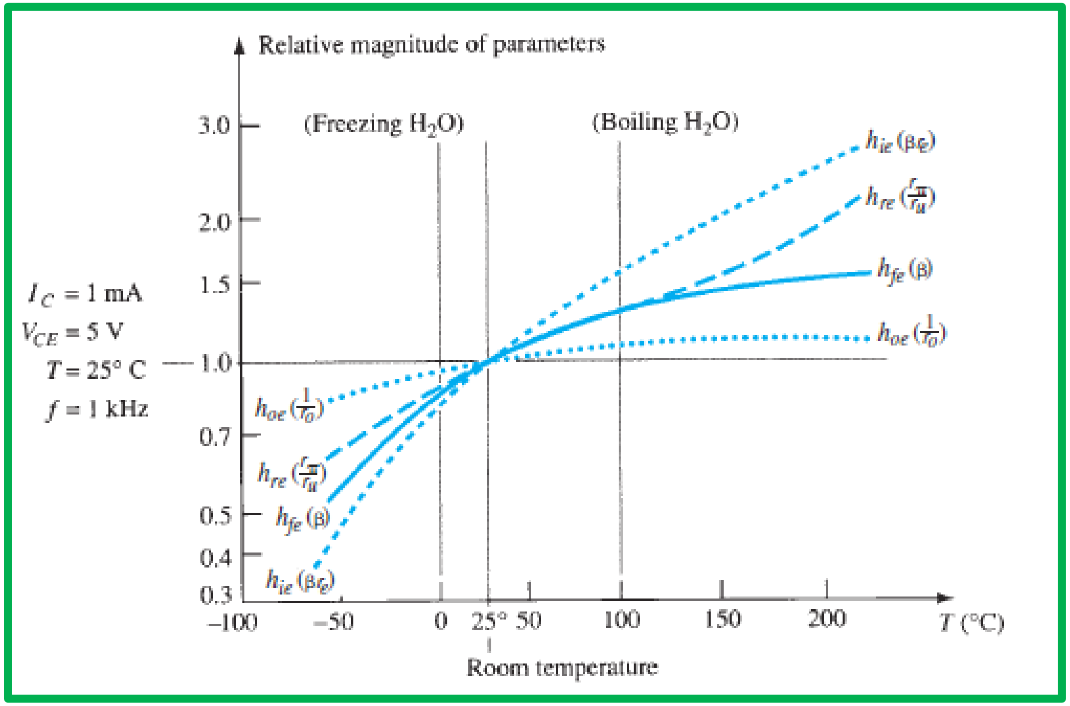


Figure 5.50: Hybrid parameter variations with temperature.

5.14 Variations of BJT Parameters Cont'd

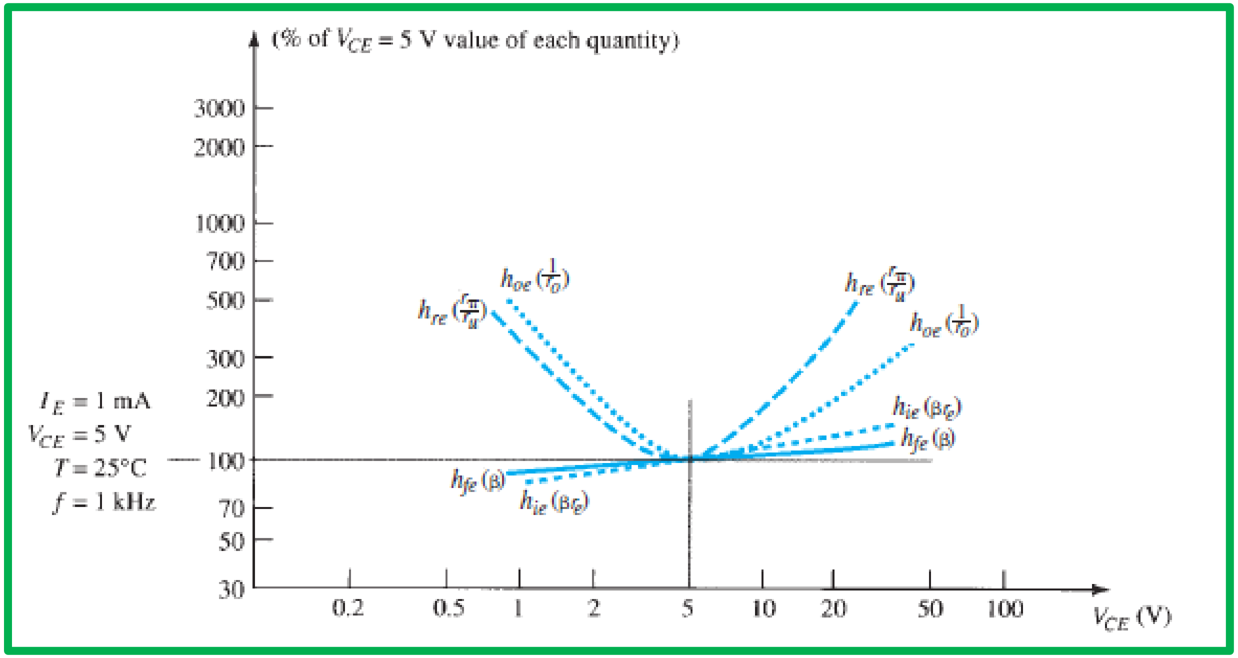


Figure 5.51: Hybrid parameter variations with collector-emitter voltage.

End of Lecture 5

Thank you for your attention!