EEE3571 Electronic Engineering I

Lecture 7: Field Effect Transistors DC Biasing and Small-signal Analysis

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References

Our main reference text books in this course are

[1] Neil S., Electronics: A Systems Approach, 4th edition, 2009, Pearson Education Limited, ISBN 978-0-273-71918-2.

[2] Boylestad R. L., Nashelsky L., Electronic Devices and Circuit Theory, 11th Ed, 2013, Prentice-Hall, ISBN 978-0-13-262226-4.

[3] Smith R. J., Dorf R. C., Circuits Devices and Systems, 5th Ed., 2004, John Wiley, ISBN ISBN 9971-51-172-X.

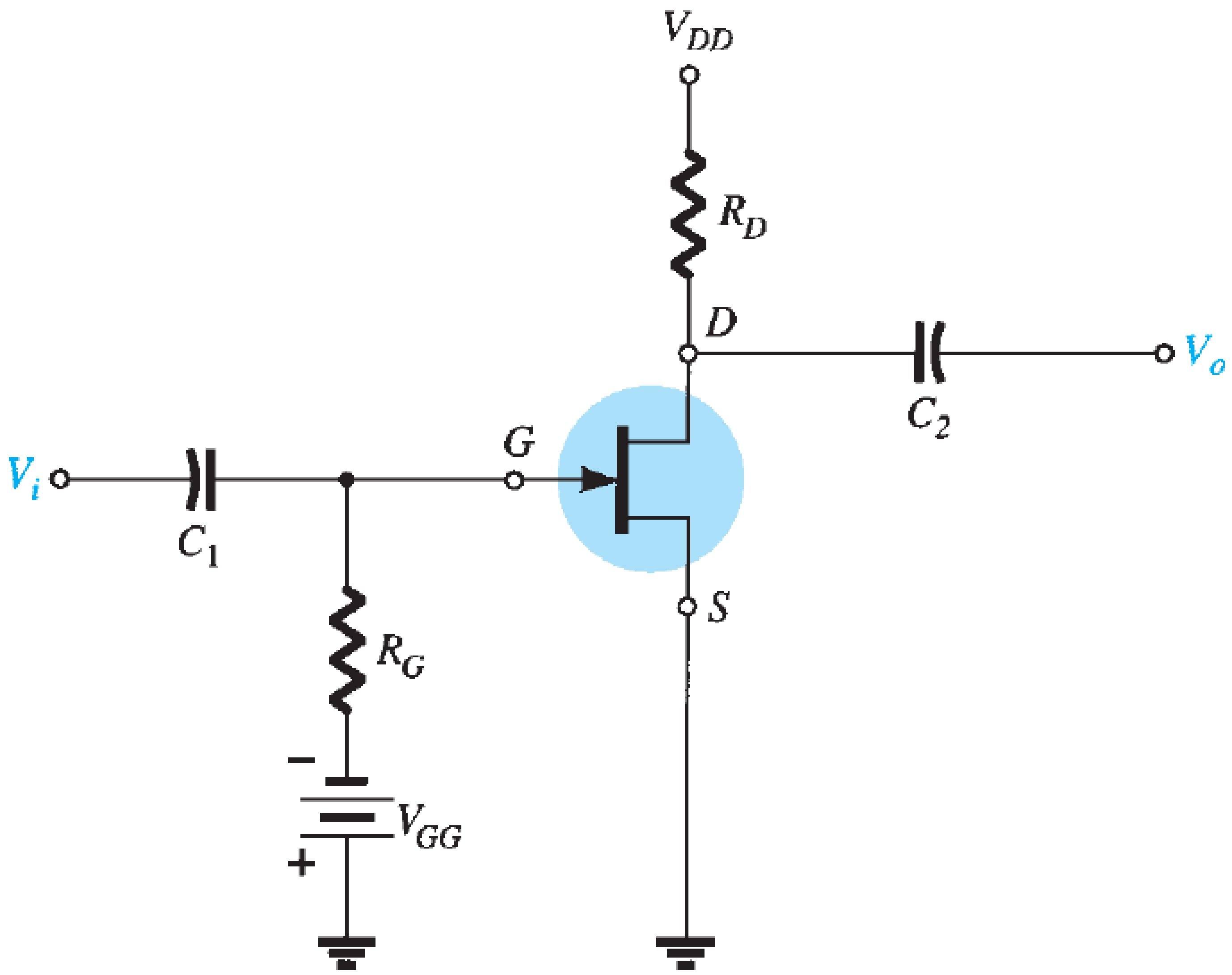
However, feel free to use pretty much any additional text which you might find relevant to our course.

Learning Objectives

At the end of this, you ought to:

1) Be able to compute the bias points of JFETs for the following configurations:
    1) Fixed bias and
    2) Voltage-divider configuration.
2) Be able to compute the bias points of E-MOSFETs for the Voltage divider configuration.
3) Be introduced to the small-signal model for E-MOSFETS and thus be able to compute ac-parameters for a potential-divider bias based E-MOSFET amplifier.

JFET fixed-bias configuration



JFET fixed-bias configuration

EXAMPLE 7.1 Determine the following for the network of Fig. 7.6:

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_D.
e. V_G.
f. V_S.

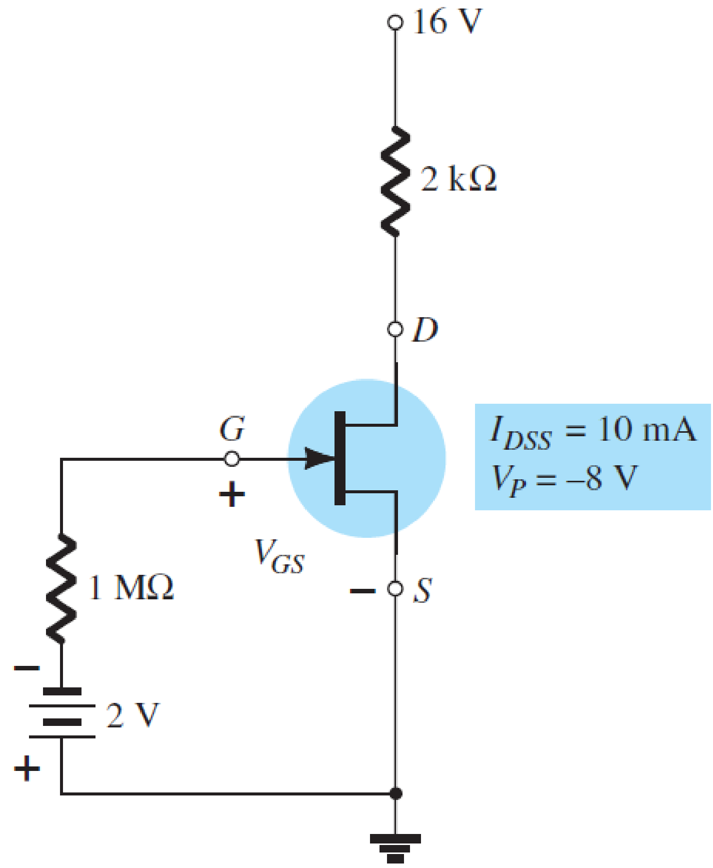


FIG. 7.6
Example 7.1.

Solution:

Mathematical Approach

a. $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

b. $$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{-2\text{ V}}{-8\text{ V}}\right)^2$$
$$= 10\text{ mA}(1 - 0.25)^2 = 10\text{ mA}(0.75)^2 = 10\text{ mA}(0.5625)$$
$$= \mathbf{5.625\ mA}$$

c. $$V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.625\text{ mA})(2\text{ k}\Omega)$$
$$= 16\text{ V} - 11.25\text{ V} = \mathbf{4.75\ V}$$

d. $V_D = V_{DS} = \mathbf{4.75\ V}$

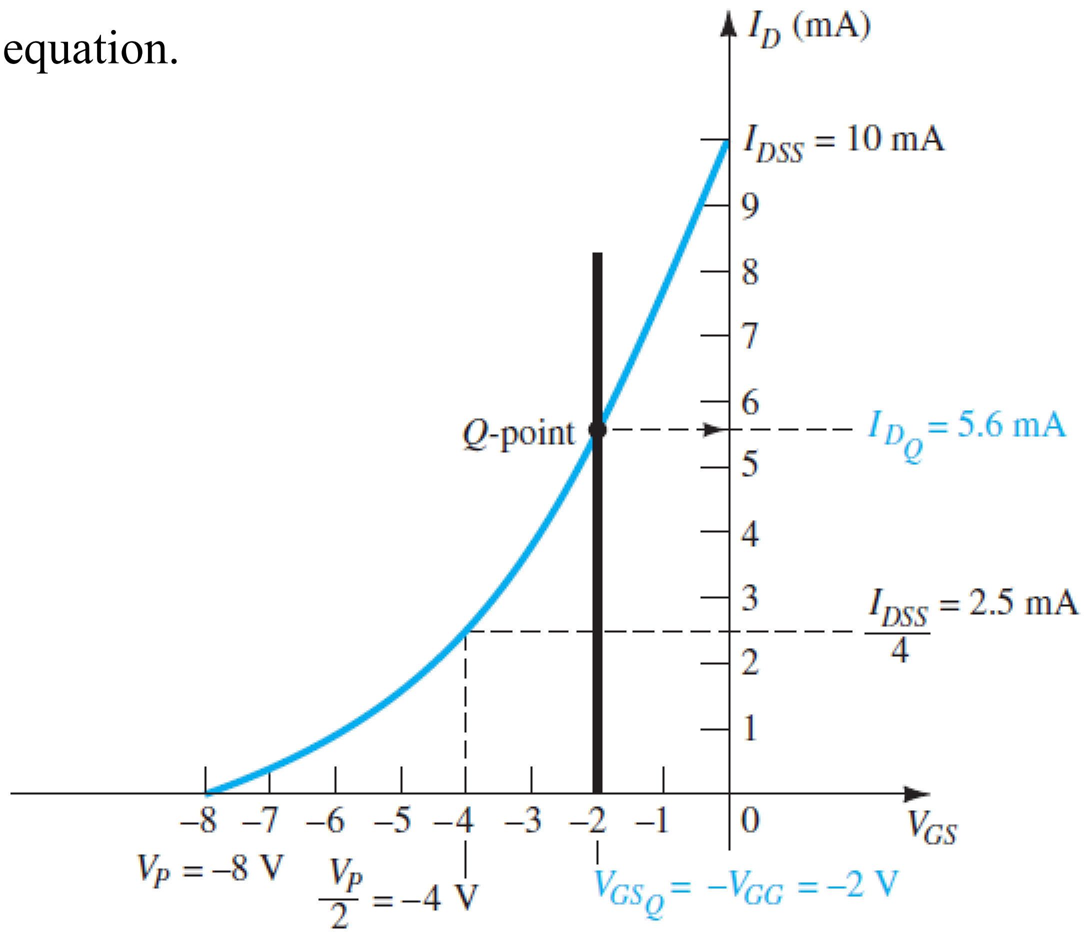
e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$

JFET fixed-bias configuration

Graphical Approach

Plot using Shockley's equation.



JFET fixed-bias configuration

Graphical Approach

a. Therefore,

$$V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$$

b. $I_{D_Q} = \mathbf{5.6\ mA}$

c. $V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.6\text{ mA})(2\text{ k}\Omega)$
$\quad = 16\text{ V} - 11.2\text{ V} = \mathbf{4.8\ V}$

d. $V_D = V_{DS} = \mathbf{4.8\ V}$

e. $V_G = V_{GS} = \mathbf{-2\ V}$

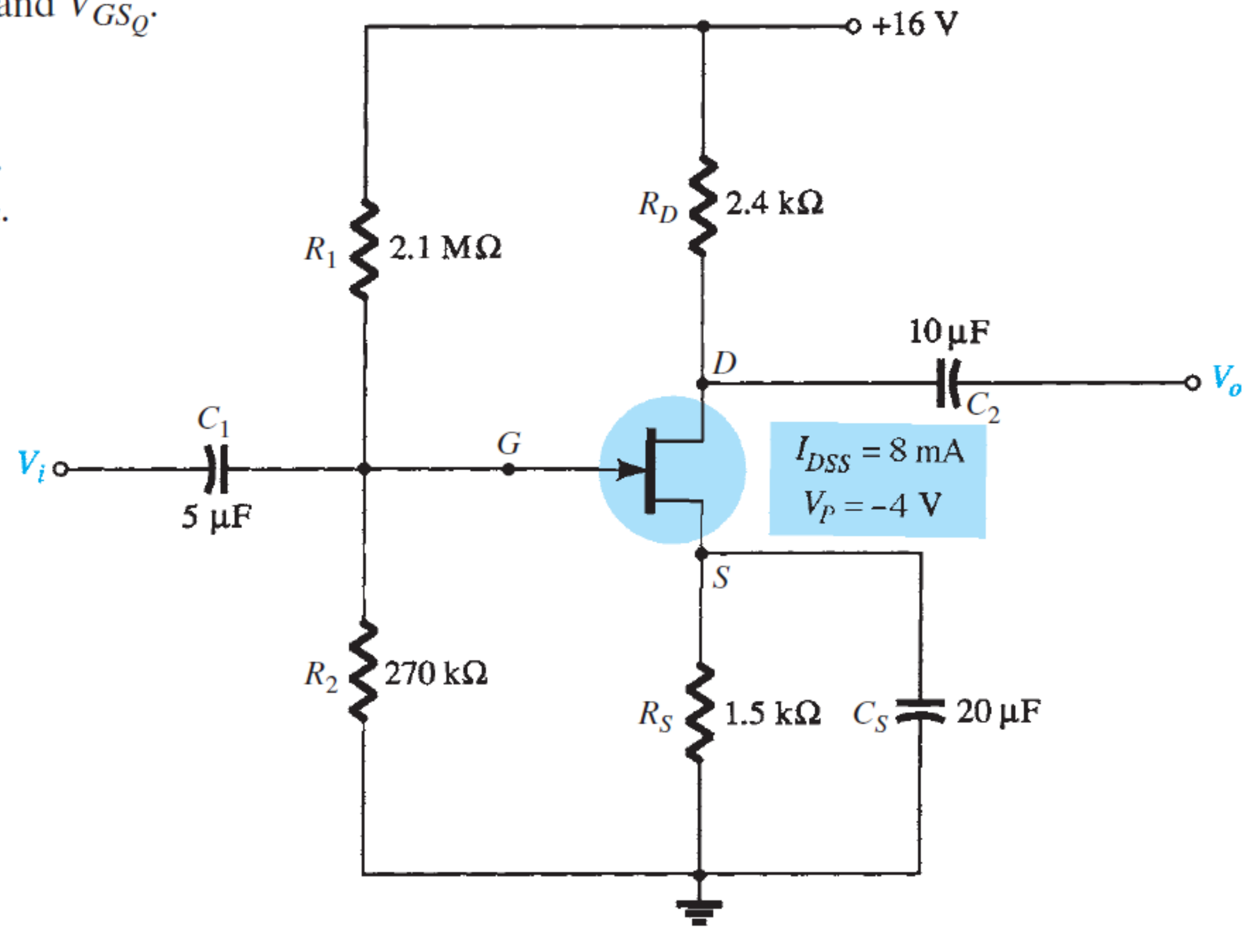
f. $V_S = \mathbf{0\ V}$

The results clearly confirm the fact that the mathematical and graphical approaches generate solutions that are quite close.

JFET Voltage-divider biasing

EXAMPLE 7.4 Determine the following for the network of Fig. 7.21:

a. I_{D_Q} and V_{GS_Q}.
b. V_D.
c. V_S.
d. V_{DS}.
e. V_{DG}.



JFET Voltage-divider biasing

a. For the transfer characteristics, if $I_D = I_{DSS}/4 = 8\text{ mA}/4 = 2\text{ mA}$, then $V_{GS} = V_P/2 = -4\text{ V}/2 = -2\text{ V}$. The resulting curve representing Shockley's equation appears in Fig. 7.22. The network equation is defined by

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$= \frac{(270\text{ k}\Omega)(16\text{ V})}{2.1\text{ M}\Omega + 0.27\text{ M}\Omega}$$

$$= 1.82\text{ V}$$

and

$$V_{GS} = V_G - I_D R_S$$

$$= 1.82\text{ V} - I_D(1.5\text{ k}\Omega)$$

When $I_D = 0\text{ mA}$,

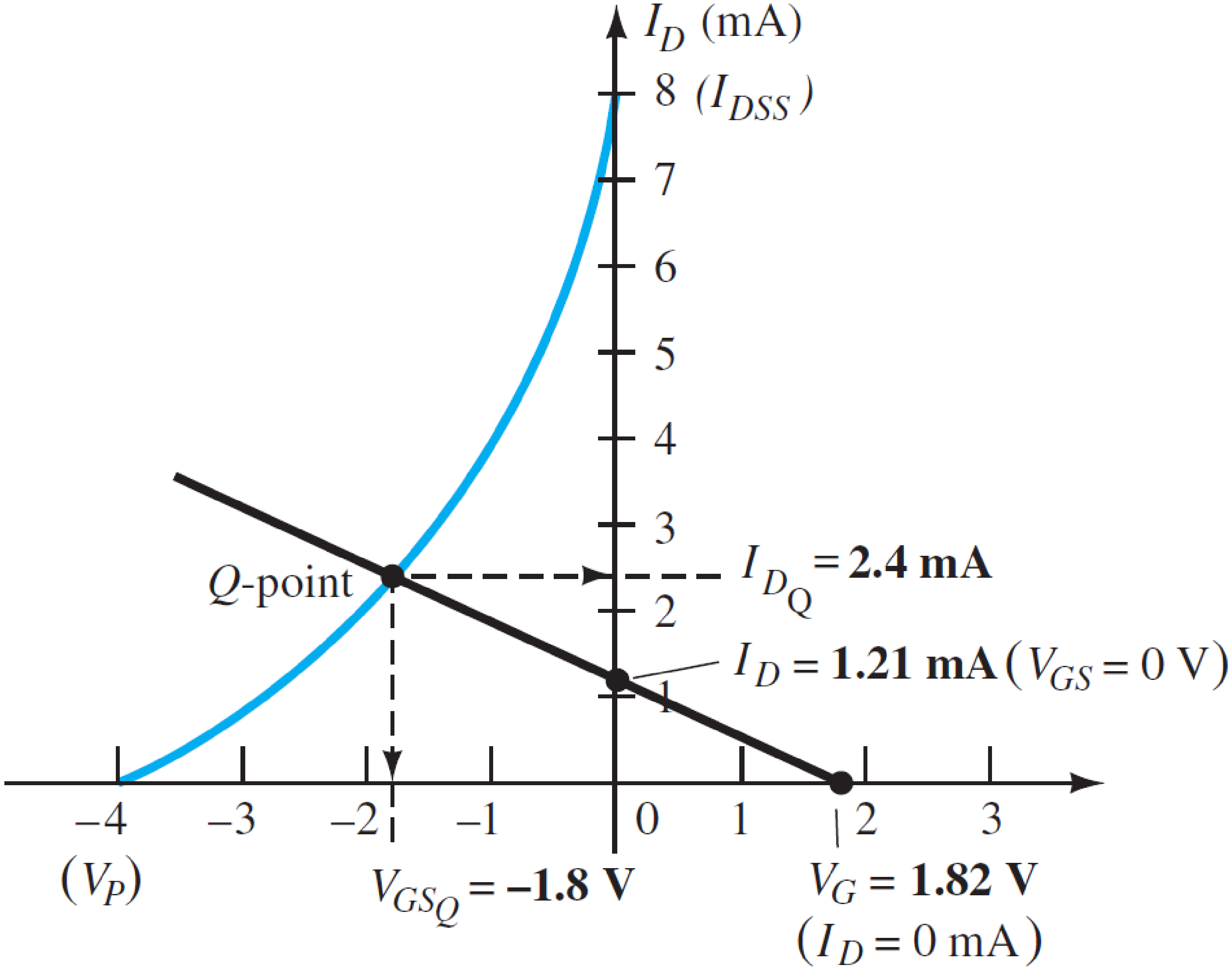
$$V_{GS} = +1.82\text{ V}$$

When $V_{GS} = 0\text{ V}$,

$$I_D = \frac{1.82\text{ V}}{1.5\text{ k}\Omega} = 1.21\text{ mA}$$

We then plot the input characteristics and the straight line from KVL on the input on the same axis to determine the intersection point.

JFET Voltage-divider biasing



JFET Voltage-divider biasing

b. $V_D = V_{DD} - I_D R_D$

$= 16\ \text{V} - (2.4\ \text{mA})(2.4\ \text{k}\Omega)$

$= \mathbf{10.24\ V}$

c. $V_S = I_D R_S = (2.4\ \text{mA})(1.5\ \text{k}\Omega)$

$= \mathbf{3.6\ V}$

d. $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 16\ \text{V} - (2.4\ \text{mA})(2.4\ \text{k}\Omega + 1.5\ \text{k}\Omega)$

$= \mathbf{6.64\ V}$

or $V_{DS} = V_D - V_S = 10.24\ \text{V} - 3.6\ \text{V}$

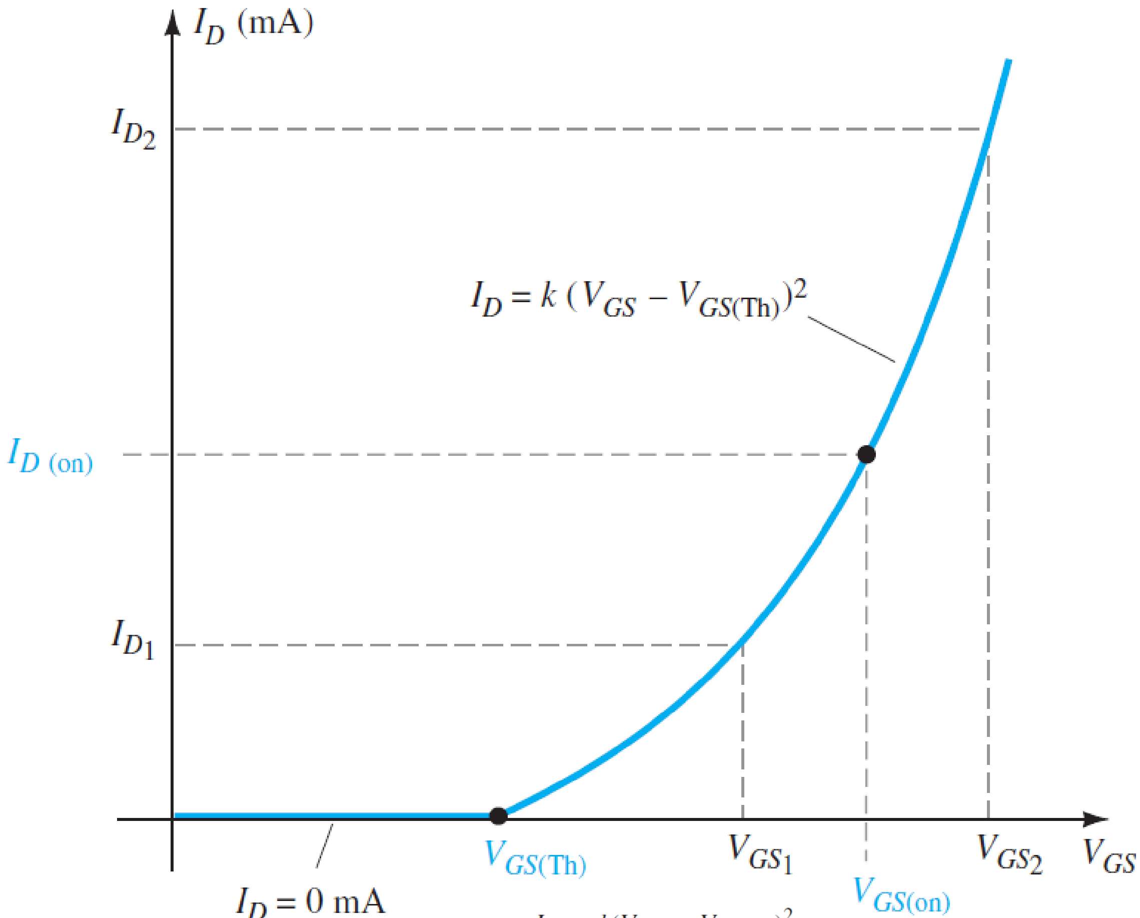
$= \mathbf{6.64\ V}$

Biasing of Depletion-Type MOSFETs

- Generally the same procedure used to determine the operating point of JFETs is used for depletion-type MOSFETS consequently they will not be covered here.
- Kindly see examples and questions in the prescribed textbook.

Voltage-divider biasing for Enhancement-Type MOSFETs

- The transfer characteristics of the enhancement-type MOSFET are quite different from those encountered for the JFET and depletion-type MOSFETs,
- The transfer function is given by:



$$I_D = k(V_{GS} - V_{GS(\mathrm{Th})})^2$$

Where, $I_{D(\mathrm{on})} = k(V_{GS(\mathrm{on})} - V_{GS(\mathrm{Th})})^2$

Voltage-divider biasing for Enhancement-Type MOSFETs

EXAMPLE 7.11 Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the network of Fig. 7.44.

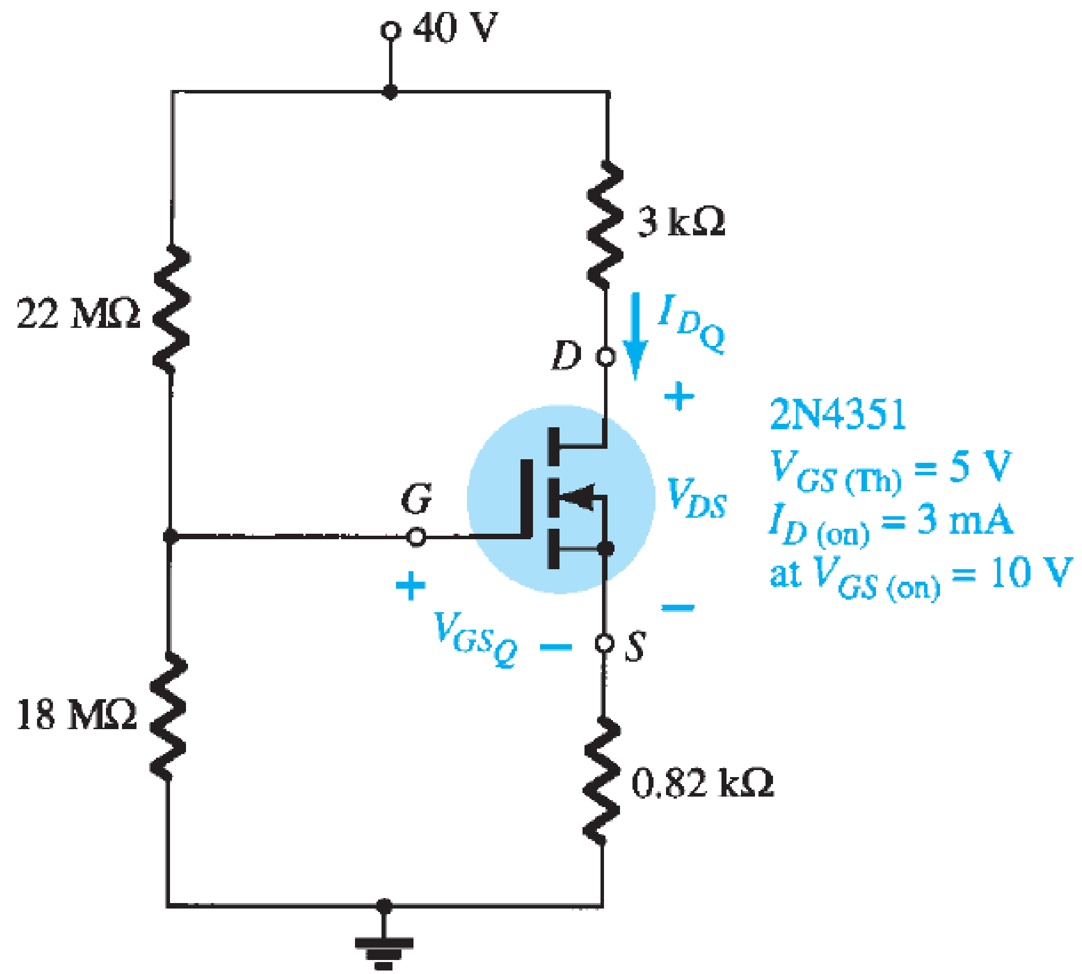


FIG. 7.44

Voltage-divider biasing for Enhancement-Type MOSFETs

EXAMPLE 7.11 Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the network of Fig. 7.44.

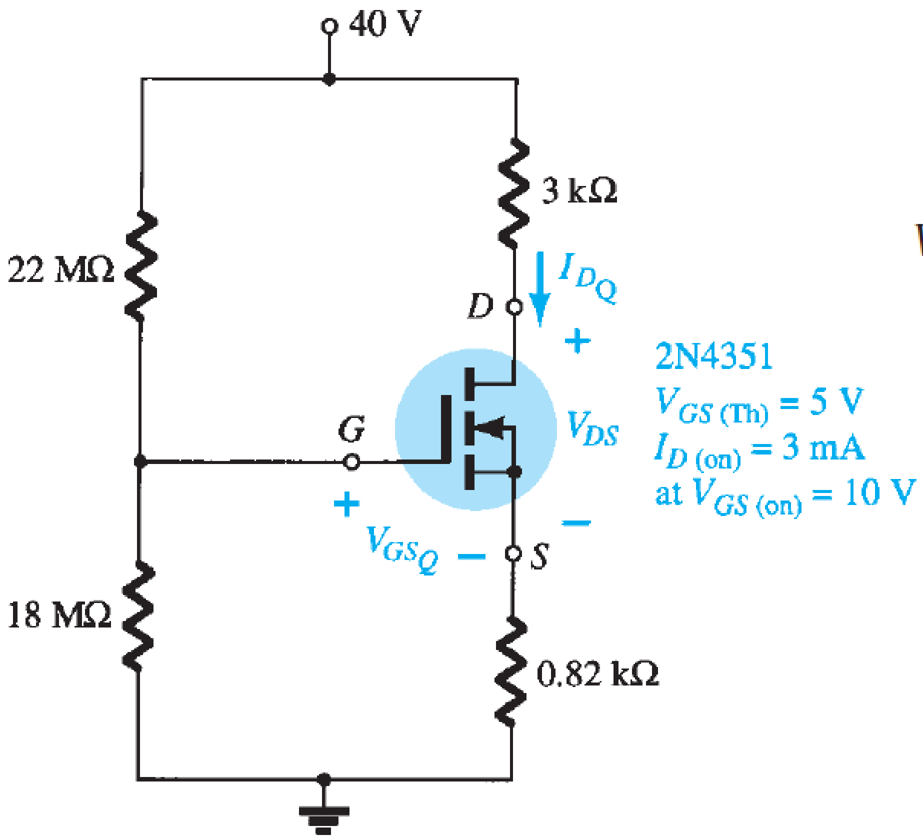


FIG. 7.44

Network

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\text{ M}\Omega)(40\text{ V})}{22\text{ M}\Omega + 18\text{ M}\Omega} = 18\text{ V}$$

$$V_{GS} = V_G - I_D R_S = 18\text{ V} - I_D(0.82\text{ k}\Omega)$$

When $I_D = 0$ mA,

$$V_{GS} = 18\text{ V} - (0\text{ mA})(0.82\text{ k}\Omega) = 18\text{ V}$$

When $V_{GS} = 0$ V,

$$V_{GS} = 18\text{ V} - I_D(0.82\text{ k}\Omega)$$

$$0 = 18\text{ V} - I_D(0.82\text{ k}\Omega)$$

$$I_D = \frac{18\text{ V}}{0.82\text{ k}\Omega} = 21.95\text{ mA}$$

Voltage-divider biasing for Enhancement-Type MOSFETs

EXAMPLE 7.11 Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the network of Fig. 7.44.

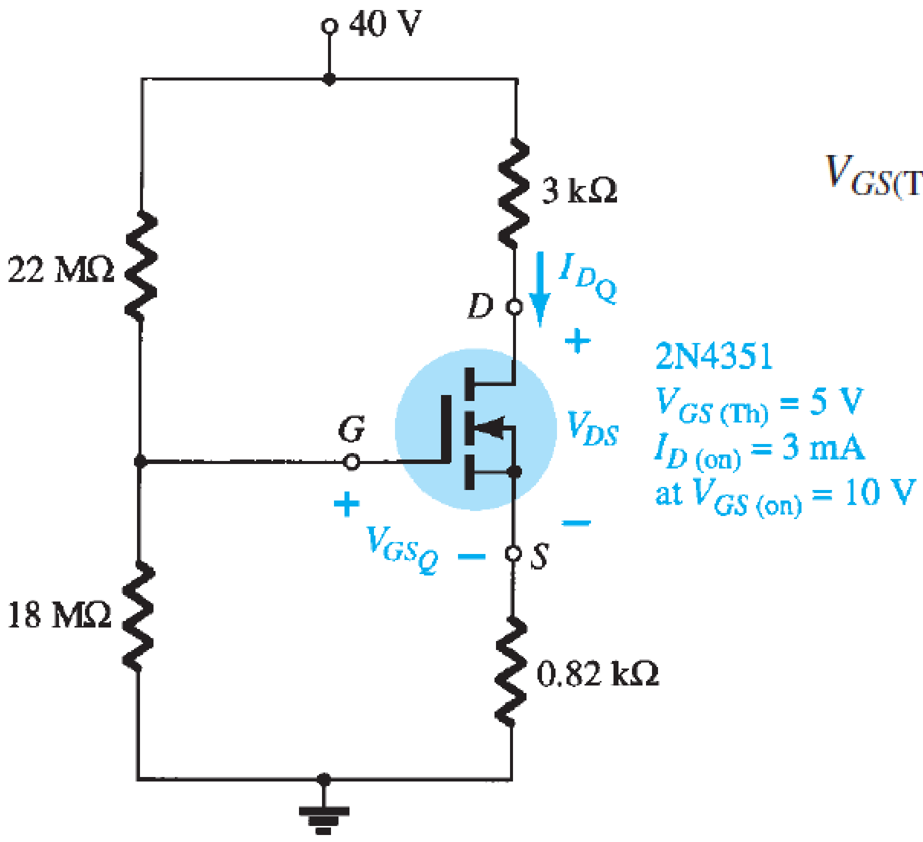


FIG. 7.44

Device

$$V_{GS(\text{Th})} = 5\text{ V}, \qquad I_{D(\text{on})} = 3\text{ mA with } V_{GS(\text{on})} = 10\text{ V}$$

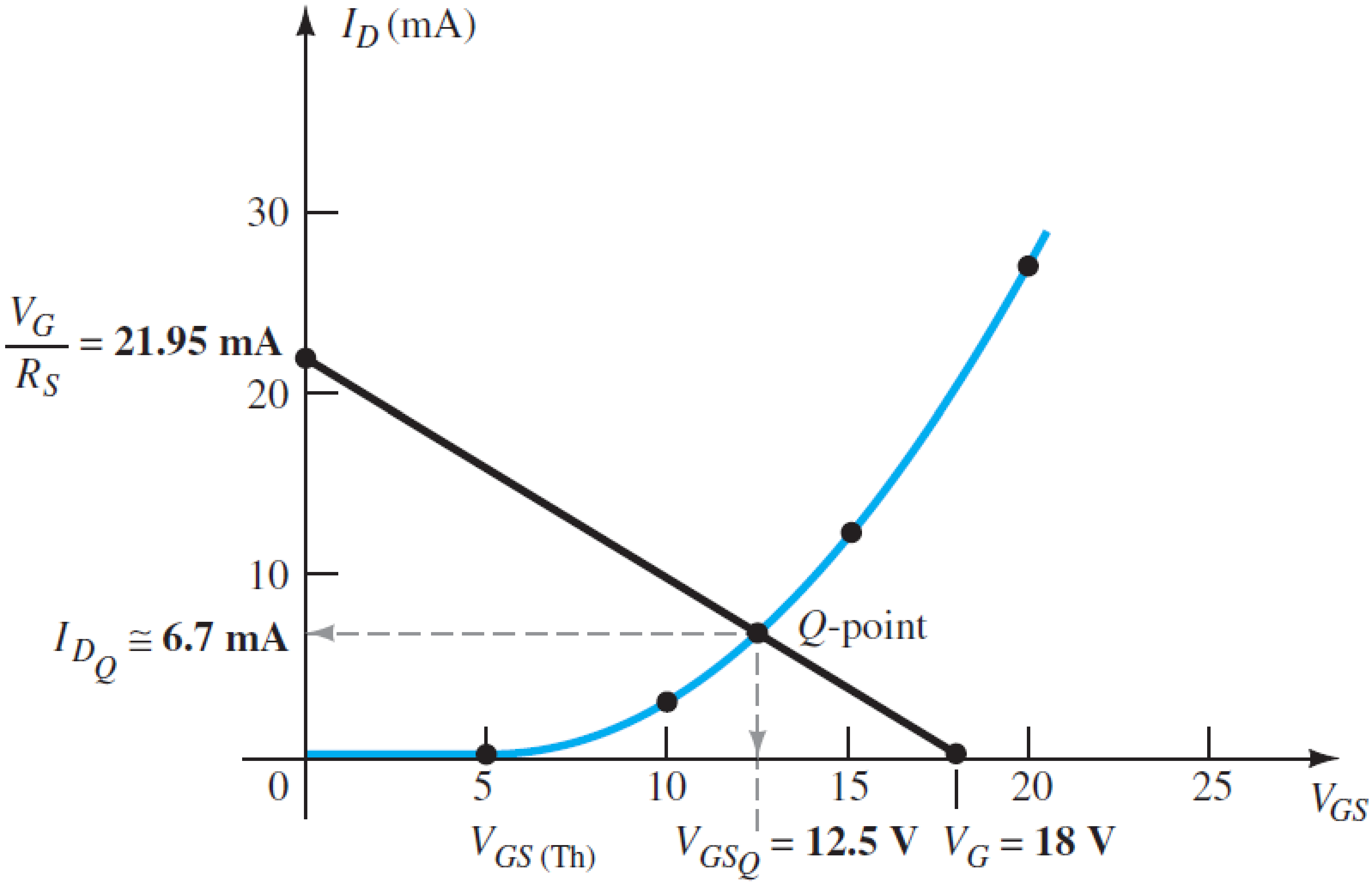
$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2} = \frac{3\text{ mA}}{(10\text{ V} - 5\text{ V})^2} = 0.12 \times 10^{-3}\text{ A/V}^2$$

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2 = 0.12 \times 10^{-3}(V_{GS} - 5)^2$$

We then plot the input characteristics and the straight line from KVL on the input on the same axis to determine the intersection point.

Voltage-divider biasing for Enhancement-Type MOSFETs

EXAMPLE 7.11 Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the network of Fig. 7.44.



Voltage-divider biasing for Enhancement-Type MOSFETs

EXAMPLE 7.11 Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the network of Fig. 7.44.

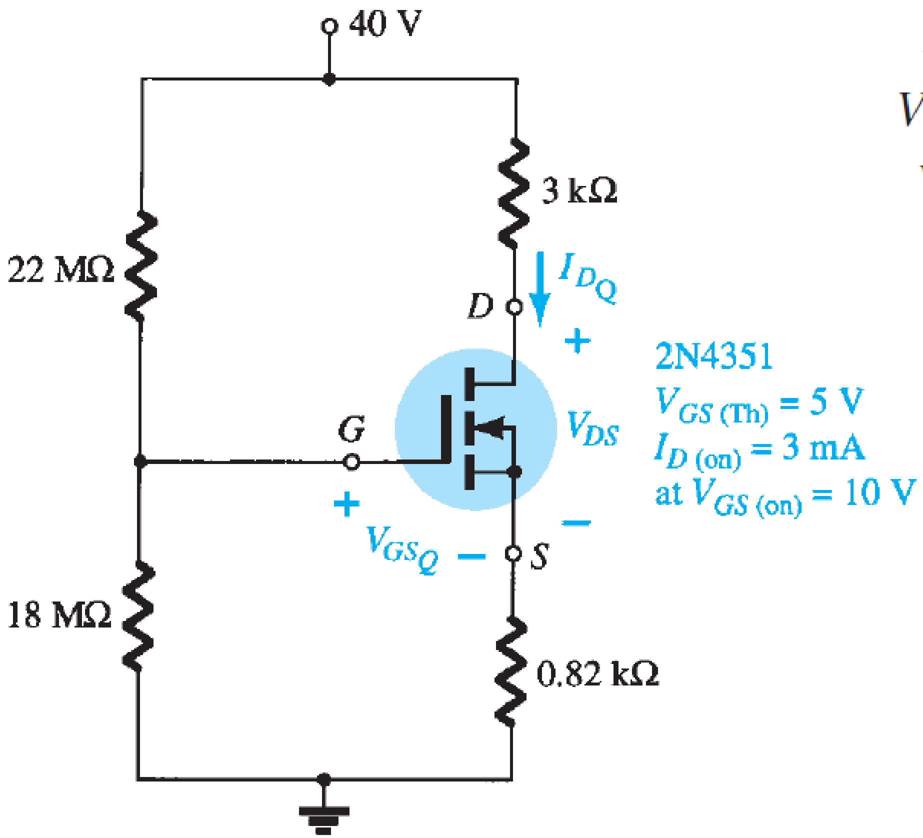


FIG. 7.44

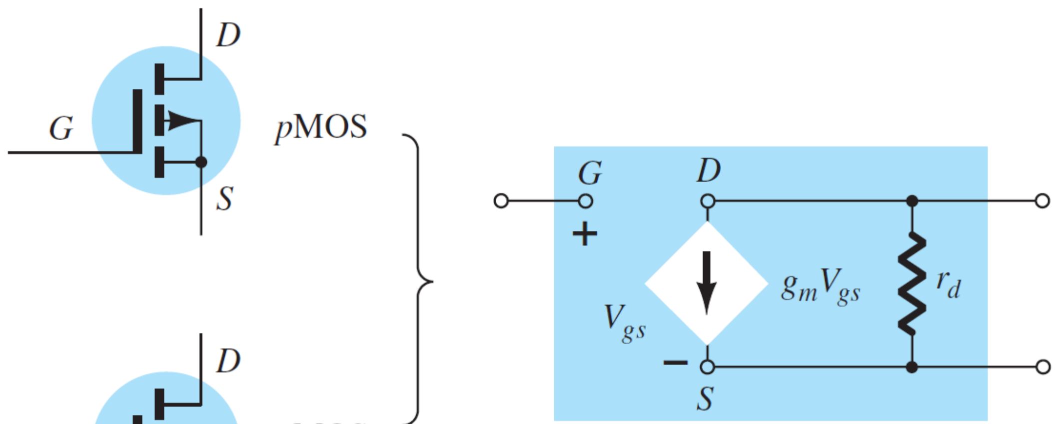
$$I_{D_Q} \cong \mathbf{6.7\ mA}$$

$$V_{GS_Q} = \mathbf{12.5\ V}$$

$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_S + R_D) \\ &= 40\text{ V} - (6.7\text{ mA})(0.82\text{ k}\Omega + 3.0\text{ k}\Omega) \\ &= 40\text{ V} - 25.6\text{ V} \\ &= \mathbf{14.4\ V} \end{aligned}$$

Small Signal Analysis Enhancement-Type MOSFETs

- E-MOSFET can be either an n-channel (*n*MOS) or *p*MOS device.
- The ac small-signal equivalent circuit has an open-circuit between gate and drain–source channel.
- A current source from drain to source having a magnitude dependent V_{GS}
- Output impedance from drain to source r_d is usually provided on specification sheets as a conductance g_{os} or admittance y_{os} .
- The device *transconductance* g_m is provided on specification sheets as the forward transfer admittance y_{fs} .



$$g_m = g_{fs} = |y_{fs}| \quad r_d = \frac{1}{g_{os}} = \frac{1}{|y_{os}|}$$

Small Signal Analysis Enhancement-Type MOSFETs

Since g_m is still defined by

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

we can take the derivative of the transfer equation to determine g_m as an operating point. That is,

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} k(V_{GS} - V_{GS(\text{Th})})^2 = k\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 2k(V_{GS} - V_{GS(\text{Th})})\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})}) = 2k(V_{GS} - V_{GS(\text{Th})})(1 - 0)$$

and

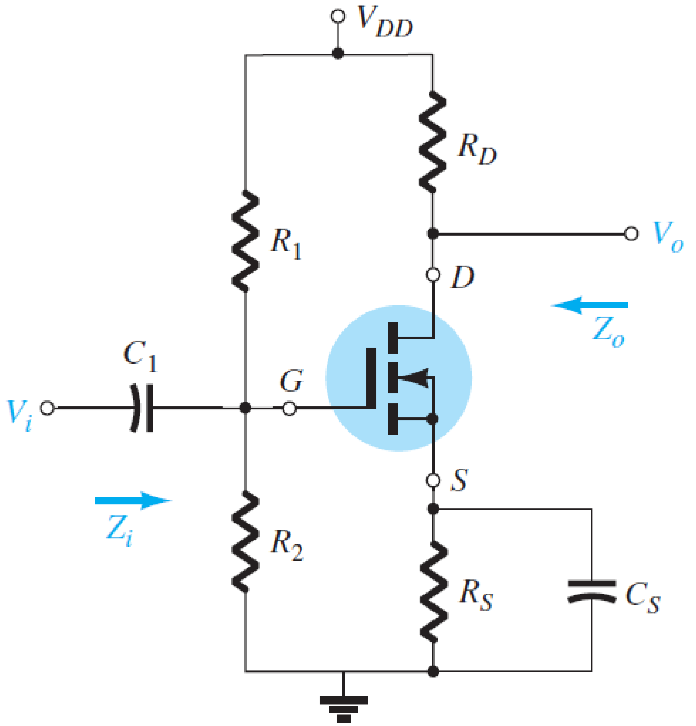
$$\boxed{g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})})} \qquad \textbf{(8.45)}$$

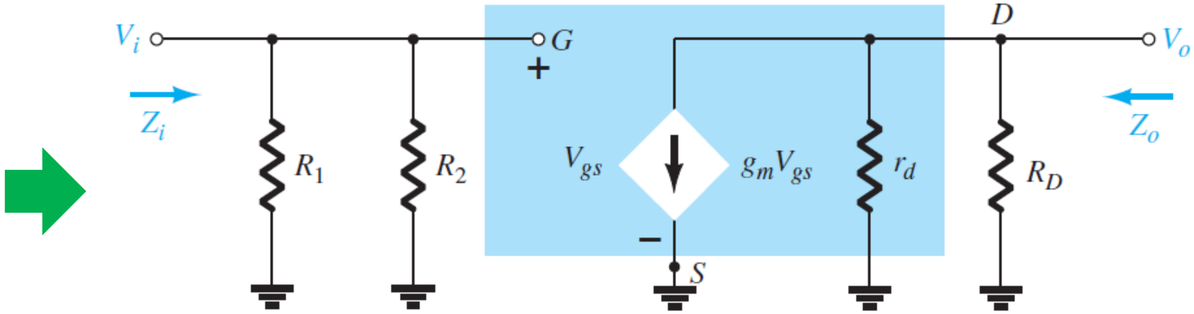
Small Signal Analysis Enhancement-Type MOSFETs

- In every other respect, the ac analysis is the same as that employed for JFETs or D-MOSFETs.
- Be aware, however, that the characteristics of an E-MOSFET are such that the biasing arrangements are somewhat limited.

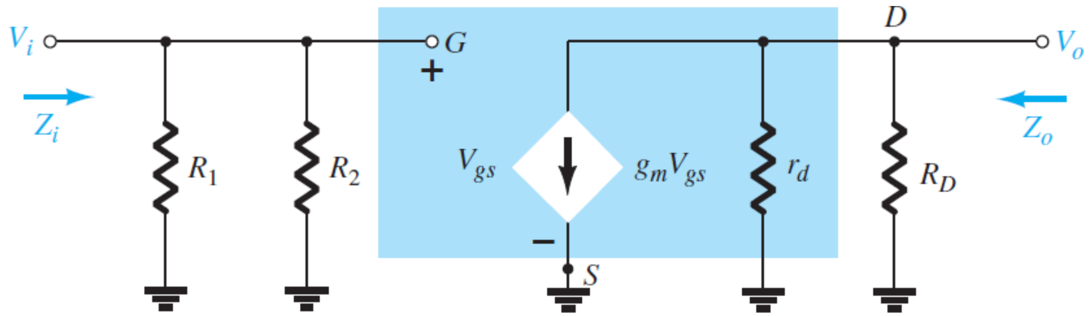
Small Signal Analysis Enhancement-Type MOSFETs

- Just as with BJTs you substitute the FET with the small-signal model and short out all capacitors and DC voltage sources.





Small Signal Analysis Enhancement-Type MOSFETs



Z_i

$$\boxed{Z_i = R_1 \| R_2}$$

Z_o

$$\boxed{Z_o = r_d \| R_D}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_d}_{r_d \geq 10R_D}$$

A_v

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)}$$

and if $r_d \geq 10R_D$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -g_m R_D}$$

End of Lecture 7

Thank you for your attention!