THE UNIVERSITY OF ZAMBIA

SCHOOL OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

UNIVERSITY EXAMINATIONS

END OF 2013 ACADEMIC YEAR EXAM - July 2014

EEE 3132

DIGITAL ELECTRONICS

TIME	:	Three (3) hours
INSTRUCTIONS	:	Answer any five (5) questions
ADDITIONAL INFORMATION	:	A list of some formulas is provided at the end

QUESTION 1

a)

i) Write in 16-bit format the Excess-3 equivalent codes of 6_{10} and 537_{10}. **[4 Marks]**

ii) Convert the decimal number 27.5625 to its binary equivalent. **[3 Marks]**

b) On a Spacecraft triple sensing systems are used to increase reliability. In this system no action is taken unless at least two of the three systems call for action.

i) Construct a truth table for the spacecraft triple sensing system. Take 0 to denote 'no action' and 1 to denote 'action'. **[3 Marks]**

ii) From the truth table write the minterm (sum-of-products) Boolean expression. **[2 Marks]**

iii) Simplify the above expression using the Karnaugh map method. **[4 Marks]**

iv) By means of DeMorgan's theorem convert the simplified minterm expression to a NANDed product of NANDs expression. **[2 Marks]**

v) Draw the logic circuit for the expression obtained in (iv). **[2 Marks]**

[Total 20 Marks]

QUESTION 2

a) Subtraction in binary can be performed by addition of signed 2's complement of operands.

i) Using signed 2's complement notation, express as 8 bit words the decimal numbers 25 and -87. **[4 Marks]**

ii) Hence, perform in 2's complement notation the arithmetic operation $25-87$. **[4 Marks]**

b) A sum of products (SOP) Boolean expression in short form notation is given as $f\left(A,B,C,D,E\right)=\sum 1,5,13,17,21,25+\sum_{d} 9,26,29$, where the second summation over d denotes the 'don't care' conditions.

i) Draw the Minterm Karnaugh map for the given expression. **[8 Marks]**

ii) Using the Karnaugh map in (i) find the minimized Boolean expression. **[2 Marks]**

iii) Hence, draw the minimized logic circuit. **[2 Marks]**

[Total 20 Marks]

QUESTION 3

a)

i) Determine the octal equivalent of the decimal number 93.75. **[3 Marks]**

ii) Multiply the binary numbers 1101.01 and 10.1. **[2 Marks]**

b) The Boolean expression for a two-input OR gate is given by $Y = A + B$, where A and B are input logic variables and *Y* the output.

i) With the aid of appropriate Boolean laws and theorems modify the given expression so as to implement a two-input OR gate using two-input NAND gates only.

[3 Marks]

ii) Hence, draw the logic circuit implementation of a two-input OR gate using two-input NAND gates only. **[3 Marks]**

c) Given a product of sums (POS) Boolean expression in short form notation as $f(A,B,C,D) = \prod 0,2,5,7,8,10,13,15,$

i) Write the Boolean expression in its expanded form. **[3 Marks]**

ii) Draw the product of sums Karnaugh map. **[4 Marks]**

iii) Hence find the minimized Boolean expression. **[2 Marks]**

[Total 20 Marks]

QUESTION 4

a) State two advantages and two disadvantages of Emitter-Coupled Logic (ECL) in comparison with Transistor-Transistor Logic (TTL). **[4 Marks]**

b) A set of TTL NAND gates is given by the manufacturer's table that it has guaranteed **voltage output range** for logic LOW from 0V to 0.4V and for logic HIGH output is from 2.4V to 5.0V. For the inputs to these NAND gates, the recognizable HIGH level ranges from 2.0V to 5.0V while the recognizable LOW input level is from 0V to 0.8V. Calculate the noise margin and comment the significance of this quantity. **[6 Marks]**

c) The following four ICs are variants of a Quad 2-input NOR gate implemented using TTL: 7402, 74H02, 74L02 and 74LS02.

Briefly describe the performance characteristics of each of the above ICs as implied by the name/designation and how the specific performance objective is implemented for each IC.

[10 Marks]

[Total 20 Marks]

QUESTION 5

a) One important form of combinational logic is a binary decoder.

i) Construct a truth table for a 1-of-8 (3 lines to 8 lines) binary decoder. **[3 Marks]**

ii) Use AND gates and Inverters to draw a circuit implementation of the 1-of-8 decoder whose truth table you have constructed above. **[4 Marks]**

iii) Describe sufficiently an area where the above binary decoder is applied in digital computer systems. **[3 Marks]**

b)

i) By using NAND gates only, draw a Master-Slave flip-flop. **[6 Marks]**

ii) Briefly describe the operation of the Master-Slave flip-flop above. **[4 Marks]**

[Total 20 Marks]

QUESTION 6

Use combinational and sequential logic to design a sequential circuit that recognizes the input sequence **1101** and outputs a HIGH.

a) Draw the state transition diagram and assign the states in binary form. **[4 Marks]**

b) Draw the state transition table showing the Present State, Input, Next State and the Output. **[6 Marks]**

c) Write the input equations relating present state and input to the next state and the output. **[4 Marks]**

d) Draw the logic circuit implementation for the sequence detector above. **[6 Marks]**

[Total 20 Marks]

QUESTION 7

a) What is the functional difference between a program counter and a stack pointer in an **8085** microprocessor? **[4 Marks]**

b) In a Simple-As-Possible (**SAP**) computer, the Arithmetic and Logic Unit (**ALU**) only performs two arithmetic operations, addition and subtraction. List four arithmetic or logic operations that the ALU in the 8085 performs and state their Assembly language OPCODES. **[8 Marks]**

c) In the **SAP** Computer, how is addition and subtraction implemented using the same hardware? **[5 Marks]**

d) What is the function of the Tri-state switches in the **SAP** computer? **[3 Marks]**

[Total 20 Marks]

Good luck!

END OF EEE 3132 EXAMINATION